A metal/insulator tunnel transistor with 16 nm channel length

Ryouta Sasajima, Kouji Fujimaru, and Hideki Matsumura[a)]
School of Materials Science, Japan Advanced Institute of Science and Technology (JAIST), Tatsunokuchi, Ishikawa-ken 923-1292, Japan

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A nanometer transistor, metal/insulator tunnel transistor (MITT), which consists of only metal and insulator is experimentally studied. In the MITT, the Fowler–Nordheim tunneling currents through an insulator in lateral metal/insulator/metal structure are controlled by changing a voltage at a gate electrode upon the middle insulator, due to variation of tunnel-barrier thickness at the insulator. It is demonstrated that the MITT with 16 nm channel length fabricated by conventional photolithography can operate similarly to the conventional metal/oxide/semiconductor field-effect transistor with on/off ratio of current larger than 10^5. The result indicates that the MITT is a promising candidate for future switching transistors in ultralarge scale integrated circuits. © *1999 American Institute of Physics.* [S0003-6951(99)04921-9]

Improvements of ultralarge scale integrated circuits (ULSI) performance have been achieved by reducing a scale of each discrete transistors contained in ULSI by following the Dennard scaling rule.[1] However, the metal/oxide/semiconductor field-effect transistor (MOSFET) with submicron scale has physical limits for reduction due to both the short-channel effect and the existence of dispensable area for metal contacts at source/drain electrodes. In addition, a random location of dopant within a channel of transistor may bring to a limit for controlling the transistor operation. To overcome these limits and to realize even smaller transistors, a new device with a size of nanometers, operating by a novel principle, is expected.

A type of tunnel effect transistors utilizing the Fowler–Nordheim (F–N) tunneling currents, the metal/insulator tunnel transistor (MITT), has been proposed by our group in 1996,[2] and its feasibility is experimentally checked by Snow *et al.*[3] and our group.[4,5] In the MITT, the drain currents by F–N tunneling through an insulating channel are controlled by applying a gate voltage. The principle is based on changing the transmission probability of the F–N tunneling by changing the potential profile or the potential thickness of the insulator near a metal electrode. This letter is to demonstrate that the MITT with 16 nm channel length is fabricated by the conventional photolithography and that it can be operated equivalently to MOSFET.

The MITT is schematically illustrated in Fig. 1. The structure of MITT consisting of only metal and insulator is similar to that of the conventional MOSFET. The insulating region (tunnel insulator) with a nanometer length L, instead of semiconductor channel in MOSFET, is laterally formed between metal source and drain electrodes. The gate electrode is prepared over a tunnel insulator through a gate insulator. The typical advantages of MITT are summarized as follows: (1) A size of MITT can be minimized to nanoscale, since the channel length can be nanoscale and a space for metal-semiconductor ohmic contacts can be eliminated. (2) The MITT can be fabricated by much simpler fabrication processes than those of semiconductor devices, since the formation of *p-n* region is not necessary. (3) High speed operation of the order of picoseconds is expected,[2] since all signal lines and electrodes are made of metal, and the drain currents are flown by tunneling phenomena. (4) Since single-crystalline metal and insulator are not required in the MITT, the three-dimensional multilayer circuits can be easily fabricated by stacking many two-dimensional circuits of MITT. (5) The operation of the MITT is not influenced from the random location of dopant, but depend on only the length of channel.

The potential profile across the metal source/tunnel-insulator/metal drain of MITT is illustrated in Fig. 2. The notation ϕ_B and E_F refer to the barrier height and the Fermi energy, respectively. When the gate electrode is positively biased toward the source electrode, the potential profile at the source/insulator interface is distorted to make the effective barrier thickness even thinner as shown in Fig. 2. On the other hand, when the gate electrode is negatively biased, the effective barrier thickness becomes thicker. It is known that the F–N tunneling currents are strongly affected by the effective barrier thickness through which electrons have to pass. Therefore, the F–N tunneling currents can be controlled through the change of effective barrier thickness by applying a gate voltage.

Moreover, the F–N tunneling currents are also changed exponentially by the variation of barrier height ϕ_B. When ϕ_B is large, on-state currents of MITT becomes small. However, when ϕ_B is small, the Schottky currents due to the

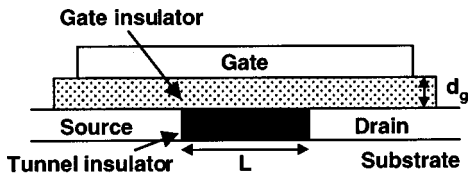

FIG. 1. Schematic diagram of the structure of a metal/insulator tunnel transistor.

a)Electronic mail: h-matsu@juist.ac.jp

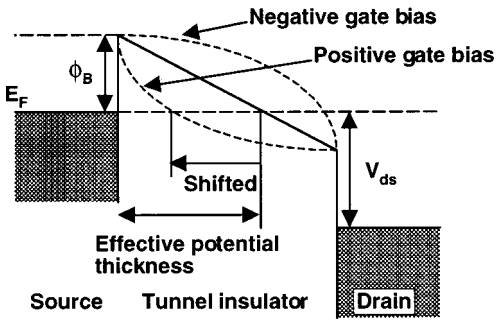

FIG. 2. Schematic view of the potential profile across the source/tunnel insulator/drain of the MITT.

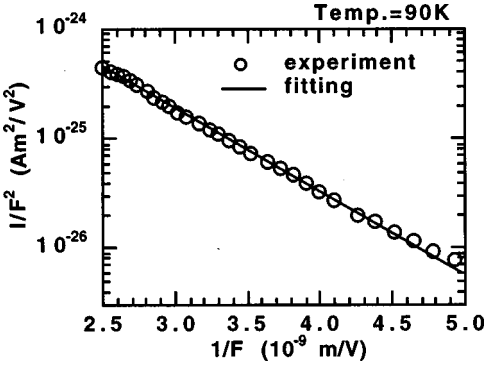

FIG. 4. Fowler–Nordheim plots of the Ti/TiO_x/Ti diode.

thermal activation of electrons over the barrier are not negligible. The Schottky currents are regarded as a noise in the MITT, because it cannot be controlled by the gate voltage. From our previous theoretical study,[2] it is found that the optimum barrier height should be around 0.6 eV for the operation of the MITT at room temperature.

The MITT with 16 nm channel length is fabricated by following processes demonstrated in Fig. 3. In the fabrication process, the conventional photolithography is used for patterning. (1) A *n*-type Si substrate is used for gate electrode and the gate insulator SiO_2 is formed by thermal oxidation. (2) A Ti film is evaporated on the gate insulator and a side of the photoresist is aligned over the gate insulator by photolithography. (3) The sidewall of Ti under the photoresist is steeply cut by the reactive ion etching (RIE) using chlorine (Cl_2) and boron trichloride (BCl_3) as mixture. (4) The tunnel insulator of TiO_x is formed by anodizing the sidewall of Ti in ethyleneglycol dissolved ammonium–tetraborate. It is found from our previous experiments that the thickness of TiO_x is proportional to the anodic voltage with a relation of 2.0 nm/V.[6] (5) A Ti film is evaporated again, on both the photoresist and the anodized TiO_x. (6) A Ti film over the photoresist is removed by lift-off technology, and the fabrication is completed.

Figure 4 demonstrates the F–N plots obtained at 90 K from the currents-voltage characteristics of the lateral Ti/TiO_x/Ti structure fabricated on the quartz substrate. The width and thickness of the Ti line are 1 μm and 30 nm, respectively. The length of TiO_x is estimated to be 16 nm from the above relation of 2.0 nm/V. Experimental data and the theoretical results are demonstrated by open circles and a solid line, respectively. The theoretical line is drawn by following the relation of temperature dependence of F–N tunneling currents.[7] By using such a relation, ϕ_B is evaluated from the fitting parameters. The ϕ_B is evaluated as about 0.3 eV. The barrier height can be also estimated from temperature dependence of the Schottky currents.[5] And the value from the Schottky currents is also 0.3 eV and in good agreement with that from the tunneling currents. The barrier height affect on both on-state currents and the noise of MITT as mentioned above. According to the prediction of our previous theoretical studies,[2,4] the high on-state currents of MITT is expected under the suppression of the Schottky currents, when it is operated at 90 K.

The experimentally obtained transfer characteristics at 90 K are demonstrated in Fig. 5. In the MITT, the width and thickness of the Ti line are 1 μm and 30 nm, respectively. The length L of tunnel insulator is 16 nm and the thickness d_g of a SiO_2 gate insulator is 10 nm. The figure shows that the source-drain currents (I_{ds}) are controlled from 10^{-12} to 10^{-7} A by the gate voltage (V_g) from -4 to $+4$ V. When V_g is smaller than -2.0 V, the F–N tunneling currents are suppressed by the negative gate bias as illustrated in Fig. 2. On the other hand, when V_g is larger than 2.0 V, it is confirmed from the F–N plots of the drain currents that the F–N tunneling currents are dominant. The saturation of the drain currents for large gate voltage is due to the saturation of the

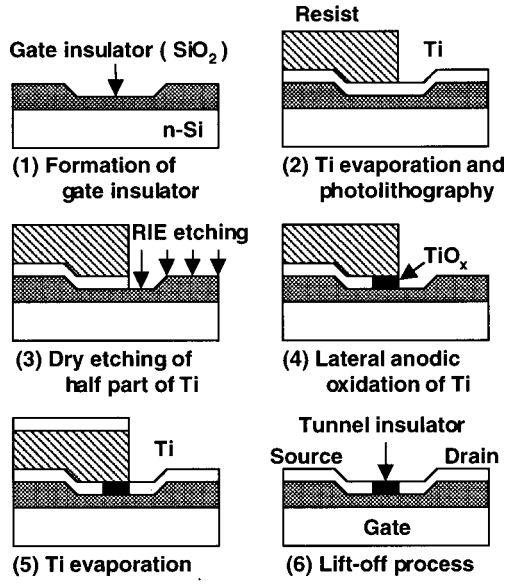

FIG. 3. Fabrication process of the MITT structure.

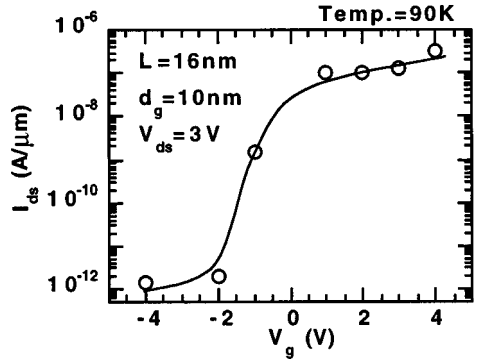

FIG. 5. Transfer characteristics of MITT.

change of gate-electric field near source electrode. It is confirmed that the gate-leakage currents of the order of picoamperes are negligible in I_{ds}. I_{ds} are clearly increased by changing the gate voltage in the orders of 10^5 enough to transfer the signal in the logic circuits.

In the present study, the MITT is operating at 90 K. If ϕ_B can be increased near to 0.6 eV, the room temperature operation would be expected due to the suppression of Schottky currents. The search of other materials apart from Ti/TiO_x system or the control of the metal/metal oxide interface is surely important for future progress.

It is concluded that the operation of MITT is similar to that of conventional MOSFET, and that the MITT is the promising candidate for the switching transistor in future ULSI because of easy fabrication process using the conventional photolithography.

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