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Description	

Nanoscale metal transistor control of Fowler–Nordheim tunneling currents through 16 nm insulating channel

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A nanoscale metal/insulator tunnel transistor (MITT) with a channel length of only 16 nm is fabricated by conventional photolithography, and its operation is experimentally studied. The MITT consists of two metal electrodes, an insulating channel inserted laterally between these two electrodes, and a third metal gate electrode formed upon the gate insulator above the insulating channel. The Fowler–Nordheim tunneling currents flowing from one metal electrode to the other through the insulating channel are controlled by applying a voltage to the gate electrode. It is found that the MITT can be operated similarly to the semiconductor transistor, and the feasibility of the nanoscale metal transistor is demonstrated. © 1999 American Institute of Physics. [S0021-8979(99)05609-1]

I. INTRODUCTION

The conventional metal/oxide/semiconductor field-effect transistor (MOSFET) has physical and technological limits for submicron fabrication.¹ Thus, a nanometer-scale transistor operating by a new principle is strongly desired to realize an even higher package density of ultralarge-scale integrated (ULSI) circuits. As one of the alternative candidates for MOSFET, the metal/insulator tunnel transistor (MITT), which consists of a metal and an insulator without a semiconductor, has been proposed by our group in 1996.²

The structure of MITT is schematically illustrated in Fig. 1. The dimensions described in Fig. 1 are used for the simulation described later. A nanometer-scale insulating region, named the tunnel insulator of length around 15 nm, is formed between the metal source and drain electrodes. Just above the tunnel insulator, the gate electrode is formed upon the gate insulator.

In the MITT, the Fowler–Nordheim (F–N) tunneling currents³ flowing through the tunnel insulator can be controlled by the gate voltage, just as in a conventional MOSFET, since the potential profile near the interface between the metal source electrode and the tunnel insulator is distorted by the electric field from the gate electrode. This is illustrated in Fig. 2, and a detailed explanation appears in the reference.² The notations ϕ_B and E_F refer to the barrier height and the Fermi energy, respectively.

When the gate electrode is positively biased toward the source electrode, the potential profile at the source–insulator interface is distorted to make the profile even sharper. It is known that F–N tunneling currents are strongly affected by the barrier width through which electrons have to pass. Thus, the F–N tunneling currents can be increased by applying a positive gate bias.

The advantages of MITT are as follows: (1) Since the channel length can be reduced to around 15 nm using F–N

tunneling currents and also since the metal electrodes are directly connected to metal-signal lines, the MITT requires only a nanoscale area for transistor action. (2) An α -ray soft error and radiation damage do not occur at all, since the MITT is made of metal and insulator without a semiconductor. (3) The MITT can be fabricated by a much simpler fabrication process than that of semiconductor devices because the formation of the p - n region is not necessary. (4) High-speed operation of the picosecond order is realized, since all signal lines and the electrodes are made of metal, and the drain currents also flow by tunneling phenomena. (5) The insulating channel of MITT is about ten times more tolerable in applying the electric field than the semiconductor channel of MOSFET, since the insulator has about ten times larger dielectric strength than the semiconductor. This is useful for nanoscale devices. (6) In the MITT, it is easy to fabricate three-dimensional circuits by stacking two-dimensional ones, since the MITT does not require the use of crystalline materials in the fabrication process.

Recently, a new technology using the tip of scanning tunnel microscopy has been reported for the fabrication of nanometer-scale devices.^{4,5} Snow *et al.*⁶ succeeded in fabricating the MITT by this technology, based on our previous suggestion.² Their work is useful in checking the fundamental physics in device operation. However, the technology does not appear to be industrially acceptable. Thus, the fabrication of MITT by conventional technology such as photolithography is strongly required.

The purpose of this study is to demonstrate the validity of our proposal regarding the MITT through its fabrication using industrially acceptable technology. The MITT with a channel length of 16 nm is fabricated by conventional photolithography only and its operation is verified. The results clearly demonstrate that the size of the transistor can be drastically minimized to the ten-nanometer scale by using the MITT instead of semiconductor transistors. Moreover, the MITT can be fabricated by a simple method because the formation of a p - n region is not necessary.

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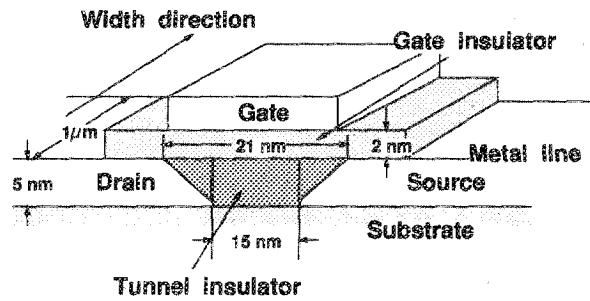


FIG. 1. Schematic view of structure of MITT.

II. RESULTS OF SIMULATION

The characteristics of MITT have been simulated based on the dimensions described in Fig. 1 to confirm the feasibility of this transistor. This has already been reported;² however, for convenience, typical results are briefly summarized here. In this example, the MITT with a tunnel insulator of 15 nm length and a gate insulator of 2 nm thickness is formed in the metal-signal line of 5 nm thickness and 1 μm width.

The transfer characteristics at room temperature are shown in Fig. 3 for $\phi_B = 0.6$ eV. The dielectric constants of the gate insulator and the tunnel insulator are 3.9 and 5.0, respectively.² When the gate voltage is smaller than 1.0 V, the Schottky currents due to the electrons activated thermally over the barrier height are dominant, since the potential profile at the source-insulator interface is not sufficiently distorted. When the gate voltage is larger than 1.0 V, the F-N tunneling currents become dominant, since the potential profile is sharply distorted.

When the barrier height is high, the tunneling probability is likely to decrease and both off and on currents decrease based on the relation $j \propto \phi_B^{-1} \exp(-\phi_B^{3/2})$, where j refers to the drain currents.³ On the other hand, when the barrier height is low, the F-N tunneling currents are likely to increase, but the Schottky currents also increase at the same time by following the relation $j \propto \exp(-\phi_{B,eff}/kT)$, where $\phi_{B,eff}$, k and T refer to the effective barrier height for various electric field intensities, Boltzmann's constant and temperature, respectively. The effective barrier height includes the Schottky barrier lowering due to the mirror effect at the metal interface.⁷ Therefore, the barrier height should be properly chosen for the operation of MITT to suppress the

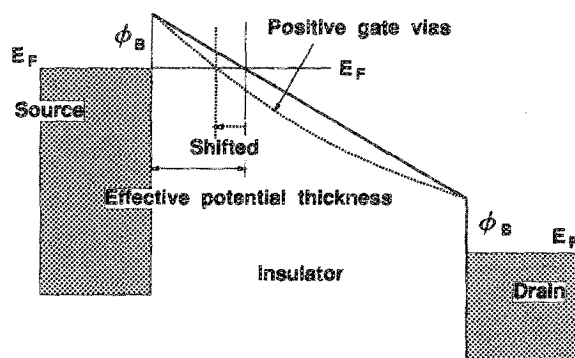


FIG. 2. Energy band diagram of source/tunnel insulator/drain in the MITT.

TABLE I. The conditions for MITT fabrication.

RIE condition	
Power of RIE	17.5 mW/cm ²
Flow rate of Cl ₂	9.0 sccm
Flow rate of BCl ₃	1.0 sccm
Gas pressure	1.0 Pa
Anodic oxidation	
Temperature of electrolyte solution	25 °C
pH of electrolyte solution	6.9

Schottky leakage currents. When the barrier height between the tunnel insulator and metal electrodes is 0.6 eV, the drain currents can be controlled in the range from 10⁻¹¹ to 10⁻⁶ A for the variation of gate voltage from 0 to 2 V, as shown in Fig. 3.

III. EXPERIMENTAL PROCEDURE

A. Selection of metal and insulator

In the present experiment, titanium (Ti) is used for the metal electrodes. Ti can adhere to the insulating substrates such as quartz. Thus, the Ti film can withstand for the fabrication process of MITT. Additionally, since the evaporated Ti film is flat in the nanoscale level, the tunnel insulator is formed exactly over the gate electrode without making pinholes.⁴

Titanium oxide (TiOx), which is prepared by anodizing Ti, and silicon nitride (SiNx) are used for the tunnel insulator and the gate insulator, respectively. Since a barrier height as low as 0.6 eV at the interface between the metal electrodes and the tunnel insulator is required to operate the MITT, a material which has a low barrier height at the interface of the metal/metal-oxide insulator should be selected. The barrier height of Ti/TiOx interface is sometimes lowered by the existence of TiO or Ti₂O₃ near the Ti/TiO₂ interface. Actually, Matsumoto *et al.* succeeded in operating a single-electron

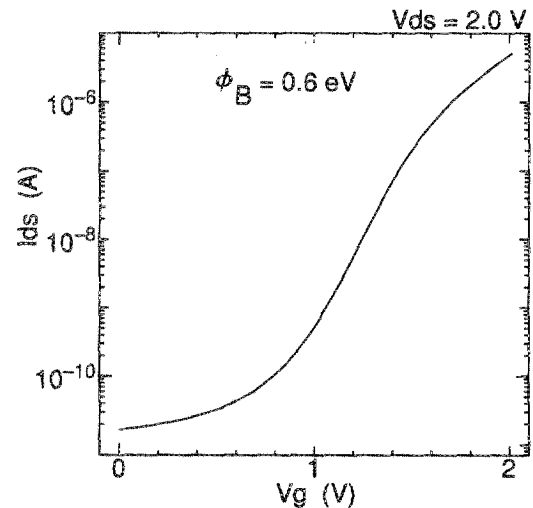


FIG. 3. Calculated results of transfer characteristics of MITT. Source-drain current I_{ds} is shown as a function of gate voltage V_g for the fixed source-drain voltage V_{ds} of 2.0 V.

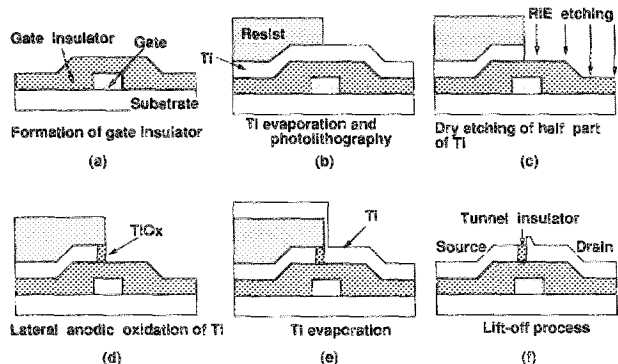


FIG. 4. Fabrication process of MITT.

transistor using the Ti/TiOx system⁸ and confirmed that the barrier height of the Ti/TiOx interface is lower than 1.0 eV.⁴ Therefore, in the present work, the MITT is fabricated using the low barrier height system of Ti/TiOx as the first step.

Other metals such as chromium and niobium (Nb), which can also adhere to the insulating substrates, have a barrier height lower than 1.0 eV at the interface of metal and metal oxide. For example, Snow *et al.* fabricated MITT using the Nb/Nb-oxide system.⁶ The material suitable for MITT is not optimized at the present time and the characteristics of MITT can be improved by choosing or finding the appropriate material.

The barrier height should be kept lower than 1.0 eV, and also the device structure which has a trapezoidal tunnel insulator as illustrated in Fig. 1 is required to improve the characteristics of MITT because of easier propagation of the electric field from the gate. Moreover, the MITT as demonstrated in Fig. 3 is expected to operate faster than the conventional MOSFET with the switching time of the picosecond order because of the small floating capacitance of the operation region. The transconductance (g_m) of MITT was also estimated to be about 1 mS/ μm from a computer simulation.² The value appears almost equivalent to that of the conventional MOSFET. Therefore, the MITT is comparable to the MOSFET.

B. Fabrication process

Figure 4 shows the fabrication process of the MITT using conventional photolithography. The MITT is fabricated as follows:^{9,10} (1) A Ti gate electrode of 1 μm width is formed on an insulating substrate such as quartz and a gate insulator of SiNx is deposited by chemical vapor deposition.¹¹ (2) A Ti film is evaporated on the gate insulator and the edge of the photoresist is aligned over the gate electrode by photolithography. (3) The sidewall of Ti under the photoresist is steeply cut by reactive ion etching using a chlorine (Cl_2) and boron trichloride (BCl_3) mixture. (4) The sidewall of Ti is anodized in ethylene glycol containing ammonium tetraborate. (5) A Ti film is evaporated again on both the photoresist and the anodized TiOx. (6) The Ti film above the photoresist is removed by lift-off technology, and finally the fabrication of MITT is completed.

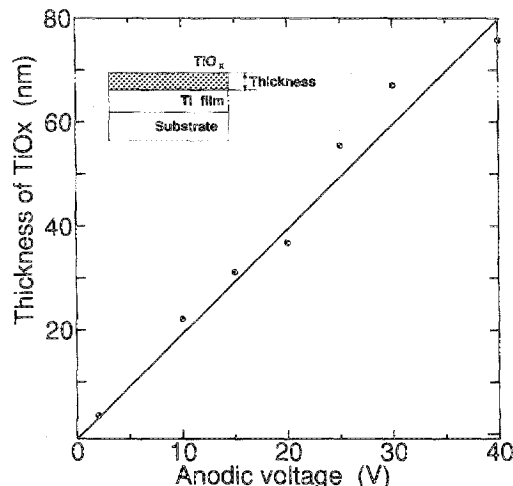


FIG. 5. Relationship between anodic voltage and TiOx thickness.

The detailed conditions for the fabrication of MITT are summarized in Table I. This fabrication process indicates the possibility of fabricating nanoscale MITT by conventional photolithography only.

C. Anodic oxidation

The tunnel insulator in MITT is formed by anodizing the sidewall of Ti. Figure 5 demonstrates the relationship between anodic voltage and TiOx thickness. The thickness of the TiOx layer grown on the surface of Ti film, as illustrated in the inset, is measured by ellipsometry using the light of a helium-neon laser. It is shown in Fig. 5 that the thickness of TiOx is proportional to the anodic voltage, keeping the relationship of 2.0 nm/V.

The relationship is evaluated from the thickness of TiOx grown vertically on the Ti film. On the other hand, the TiOx layer grown laterally by anodic oxidation at the sidewall of Ti film is utilized as the tunnel insulator. Observations by scanning electron microscopy also revealed that the thickness of the TiOx grown laterally under the photoresist exactly satisfies the same relationship of 2.0 nm/V. Therefore, the length of the tunnel insulator can be controlled by the anodic voltage.

IV. PROPERTIES OF METAL-OXIDE TUNNEL INSULATOR

A. Current-voltage characteristics

According to computer simulation, the required resistivity of the tunnel insulator is larger than $10^7 \Omega \text{ cm}$ to maintain the off-state currents lower than the Schottky leakage currents. Thus, the current-voltage (I - V) characteristics of the TiOx which is prepared in the metal-signal line by anodizing the sidewall of Ti are demonstrated to confirm the feasibility of TiOx as a tunnel insulator.

Figure 6 demonstrates the I - V characteristics of the tunnel insulator at 90 and 300 K. The width and thickness of the Ti line are 1 μm and 30 nm, respectively, as shown in the inset. The length of the tunnel insulator is estimated to be 16 nm from the anodic voltage of 8 V. It is observed that the

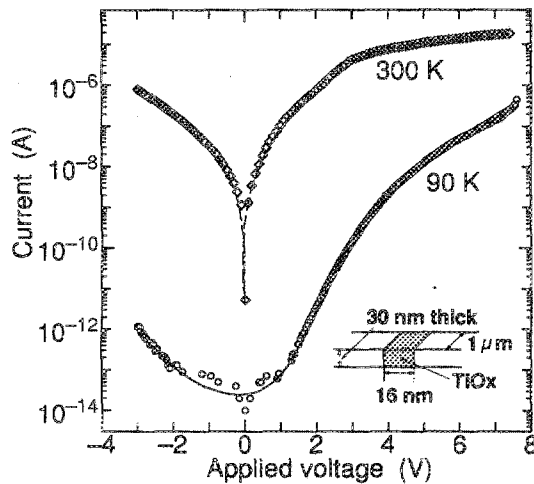


FIG. 6. I - V characteristics of the tunnel insulator.

resistivity is $3.4 \times 10^7 \Omega \text{ cm}$ at 90 K. Thus, it is confirmed that the tunnel insulator of 16 nm length, which is formed in the metal-signal line, can be realized to keep the off-state currents as low as the value estimated by the simulation.

B. Barrier height and tunneling characteristics

The barrier height between the metal electrodes and the tunnel insulator is evaluated using the temperature dependence of the leakage currents density, J_s , flowing through the tunnel insulator based on the relation $\log(J_s) \propto -\phi_{B, \text{eff}}/kT$ as mentioned earlier, if the Schottky currents are a dominant part of the leakage currents and the Poole-Frenkel currents¹² are negligible. Figure 7 shows the temperature dependence of the leakage current for various applied voltages V_a 's for the same sample as described in Fig. 6. The horizontal axis refers to the reciprocal temperature and the vertical axis refers to the leakage current through the tunnel insulator. The plots lie exactly on straight lines, that is, it is confirmed that only the Schottky currents are dominant. The slopes of the

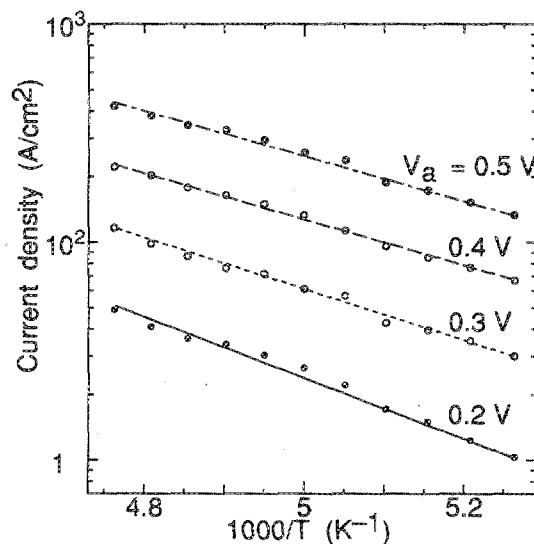


FIG. 7. Temperature dependence of the leakage current through the tunnel insulator.

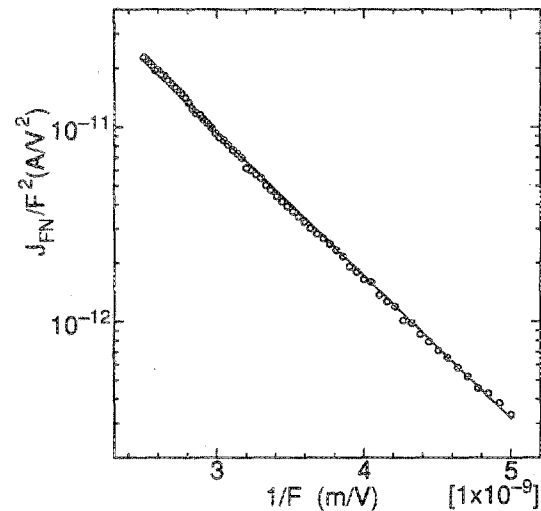


FIG. 8. F - N plots of the tunnel insulator for the electric field of 2-4 MV/cm.

plots correspond to $\phi_{B, \text{eff}}/k$. The barrier height ϕ_B is evaluated to be 0.31 eV from the relation $\phi_B = \phi_{B, \text{eff}} + \sqrt{qF/4\pi\epsilon}$, where q , F , and ϵ refer to the charge of an electron, the electric field intensity, and the permittivity, respectively. This result indicates that the appropriate barrier height to realize the high on-state currents of MITT is provided by the present system and that the increment of the leakage currents at 300 K as shown in Fig. 6 can be explained as being due to the barrier height as low as 0.31 eV.

Figure 8 demonstrates the F - N plots of the tunnel insulator obtained from the results of I - V characteristics at 90 K. The horizontal axis refers to the reciprocal electric field intensity of 2-4 MV/cm and the vertical axis refers to J_{FN}/F^2 , where J_{FN} refers to the F - N tunneling current. The plots of the F - N tunneling currents at such a low-temperature region should become a straight line with a negative gradient for $\phi_B/kT \gg 1$,¹³ since the F - N tunneling currents are expressed by $J_{FN} = AF^2 \exp(-B/F)$,³ where A and B are constants. It is confirmed that the currents through the tunnel insulator are the F - N tunneling currents. Thus, the result indicates that the F - N tunneling currents can easily flow through the tunnel insulator by applying a low electric field intensity ranging from 2 to 4 MV/cm, since the barrier height is as low as 0.31 eV.

From these results, it is found that the metal oxide formed by anodic oxidation of metals is usable as the tunnel insulator in the MITT.

V. CHARACTERISTICS OF MITT AND DISCUSSION

The experimentally obtained transfer characteristics are demonstrated in Fig. 9 at 90 K because the drain currents due to the Poole-Frenkel currents are negligible. The structure of the transistor is shown in the inset. In this particular case, the length of the tunnel insulator is 16 nm and the thickness of the gate insulator is 38 nm.

In the experiment, the gate voltage changes from 0.0 to 0.6 V while keeping the drain voltage at 0.5 V, since the gate

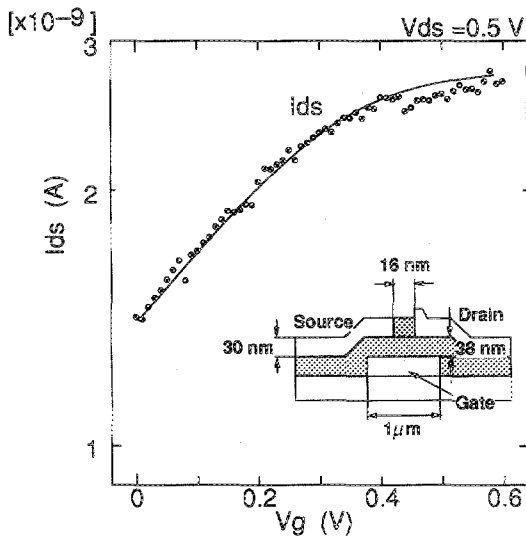


FIG. 9. Experimentally obtained transfer characteristics of MITT at 90 K.

leakage currents from the drain to the gate electrode through the gate insulator become detectable at a large drain voltage.

The drain currents are increased by increasing the gate voltage. It is confirmed that the gate-leakage currents are at least 1/10 of the drain currents and that the increment of the gate-leakage currents does not affect the drain currents. The drain currents are 10^4 times larger than that of the computer simulation of the dimensions of the fabricated transistor, the reason for which is not clear at the present time. According to recent experiments, the drain currents are likely to decrease with a slight negative bias of V_g . The potential profile in the tunnel insulator might be slightly distorted by adding the gate insulator on the Ti/TiOx/Ti lateral metal-insulator-metal diode. From the results, it is found that the switching transistor is fabricated using only a metal and an insulator and also using only conventional photolithography.

In the transfer characteristics, the variation of experimentally obtained drain currents is smaller than that expected from the computer simulation, because the thickness of the fabricated gate insulator is about 15 times that of the gate insulator used in the computer simulation described in Fig. 3. If the thickness of the fabricated gate insulator becomes 1/4, the on/off ratio is expected to become 10^5 times larger than that of the present characteristics. Actually, a recently fabricated MITT, the structure of which is slightly different from that of the present case and the thickness of gate insulator is only 10 nm, appears to operate more clearly. The results will be published in the near future.

One may doubt that this variation of the drain current occurs only by bending the band diagram of TiOx, similar to

the case of MOSFET. However, even when a strong negative bias is applied, no evidence of accumulation can be seen, and the drain currents apparently follow the F-N plots. Thus, the validity of the main concept of MITT is confirmed by the present experiments.

VI. CONCLUSIONS

From the earlier studies, the following are concluded:

- (1) Nanometer-scale metal transistors can be realized. The size of the transistors can be drastically reduced to only 16 nm using the MITT instead of semiconductor transistors.
- (2) The MITT can be fabricated by a simple method because the formation of the p - n region is not necessary, and its operation is experimentally confirmed.
- (3) The electrical characteristics of the tunnel insulator formed by anodic oxidation of metals can be used for the MITT.

These results demonstrate the feasibility of using the present new device, MITT in future applications.

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¹S. M. Sze, *Semiconductor Devices Physics and Technology* (Wiley, New York, 1985), p. 213.

²K. Fujimaru and H. Matsumura, *Jpn. J. Appl. Phys., Part 1* **35**, 2090 (1996).

³R. H. Fowler and L. Nordheim, *Proc. R. Soc. London*, **173** (1928).

⁴K. Matsumoto, M. Ishii, K. Segawa, Y. Oka, B. Vartanian, and J. Harris, *Ext. Abstr. Solid State Device and Materials*, **192** (1995).

⁵H. Sugimura, T. Uchida, N. Kitamura, and H. Masuhara, *J. Phys. Chem.* **98**, 4352 (1994).

⁶E. S. Snow, *et al.*, *Appl. Phys. Lett.* **72**, 3071 (1998).

⁷R. S. Muller and T. I. Kamins, *Device Electronics for Integrated Circuits* *Second Edition* (Wiley, New York, 1986), p. 139.

⁸K. Matsumoto, *et al.*, *Appl. Phys. Lett.* **68**, 34 (1996).

⁹K. Yamanouchi, T. Meguro, and K. Matsumoto, *IEEE Trans. Ultrason. Ferroelectr. Freq. Control* **39**, 447 (1992).

¹⁰K. Fujimaru, T. Ono, R. Nagai, and H. Matsumura, *Jpn. J. Appl. Phys., Part 1* **36**, 7786 (1997).

¹¹H. Matsumura, *Jpn. J. Appl. Phys., Part 1* **37**, 3175 (1998).

¹²J. Frenkel, *Phys. Rev.* **54**, 647 (1938).

¹³M. Koehler and I. A. Hümmelgen, *Appl. Phys. Lett.* **70**, 3254 (1997).