A Complex Baseband Platform for Spatial–Temporal Mobile Radio Channel Simulations

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***Abstract*—Recently, joint spatial–temporal signal processing has been recognized as the key to reducing the effects of the intersymbol and cochannel interference seen in very high bit-rate mobile radio communications systems. Developing hardware simulators that can simulate mobile radio propagation scenarios in time and space domains is essential for evaluating the real-time performance of spatial–temporal signal processing schemes. This paper outlines a complex baseband platform developed for spatial–temporal mobile radio channel simulations. The platform consists of a complex baseband fading/array response simulator, a digital signal processor (DSP) board, and a general-purpose parameter estimator that uses systolic array implementation of the recursive least square (RLS) algorithm. Results of experiments conducted using the developed platform are presented to confirm the proper operation of the system.**

***Index Terms*—Adaptive array, broad-band mobile communications, parameter estimation, recursive least square (RLS) algorithm, space/time-equalizer, systolic array.**

I. Introduction

MANY research papers have been published in the field of mobile multimedia communications; all target the technological breakthroughs that would enable very high bit-rate, say higher than 10 Msymbols/s, signal transmission over mobile radio channels [1], [2]. The main hurdles are the severe intersymbol interference (ISI) and cochannel interference (CCI) imposed on the received signals, due, respectively, to multipath propagation and the reuse of the same frequency in adjacent cells. Since the complex envelope of each propagation path varies as the vehicle moves, the ISI and CCI are both time-variant.

Joint space/time (S/T-) domain signal processing techniques have been recognized as effective in achieving spatial signal isolation, thereby reducing the effects of both ISI and CCI [3], [4]. Adaptive array antennas and adaptive equalization techniques, which have long been considered as constituting independent technology areas, are being combined in a unified concept that is sometimes referred to as space/time equalization [5].

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To develop S/T-equalizers and evaluate their performance, hardware simulators that can simulate spatial and temporal radio wave propagation scenarios in real-time are needed. The temporal structure of the propagation scenario can be characterized by the received signal's delay profile, and the spatial structure by the angular profile. The former can be simulated by dividing the transmitted signal into several path components corresponding to the multipaths, and weighting them appropriately. The angular profile can be simulated by rotating the signal phases of the path components received by the antenna array in accordance with their direction of arrival (DOA).

Instead of measurements in which the system to be tested, including antenna and RF/If circuitry, is placed in an anechoic chamber, the performance of time/space signal processing itself can be more conveniently evaluated by using a channel simulator connected directly to the S/T-equalizer. Since performance evaluations using such a channel simulator are not affected by the imperfections inherent within the antenna and/or RF/IF sections, higher efficiency can be expected in evaluating the performance of S/T-signal processing algorithms and optimizing their implementation.

In general, the problems inherent within S/T-equalization are twofold: one is parameter estimation, the other is sequence estimation. Parameter estimation includes problems in determining optimal weights on elements for the adaptive antenna as well as replicating received composite signal for time-domain equalization. Sequence estimation is the problem of estimating, from the S/T-equalizer output, the information sequences transmitted by the desired users.

This paper describes a hardware platform developed for spatial–temporal mobile radio channel simulations. The platform consists of a complex baseband fading/array response simulator, a DSP (Analog Devices SHARC ADSP-21 060) board, and a general-purpose parameter estimator [6] that uses systolic array implementation of the recursive least square (RLS) algorithm. The parameter estimator, which can estimate the optimal values of up to 23 parameters for S/T-equalizers, works as an adjunct to the DSP board. Obviously, the parameter estimation time is much shorter using the estimator than running the RLS algorithm on the DSP board. Data input logic configuration depends on the type of S/T-equalizer [7], so the input logic was made programmable.

The developed platform works completely in the complex baseband domain. The fading/array response simulator simulates the temporal and spatial radio wave propagation scenarios in broadband mobile communication channels in real-time. The temporal structure of the received signals can be approximated by adjusting path strengths, and the spatial structure by adjusting their DOAs.

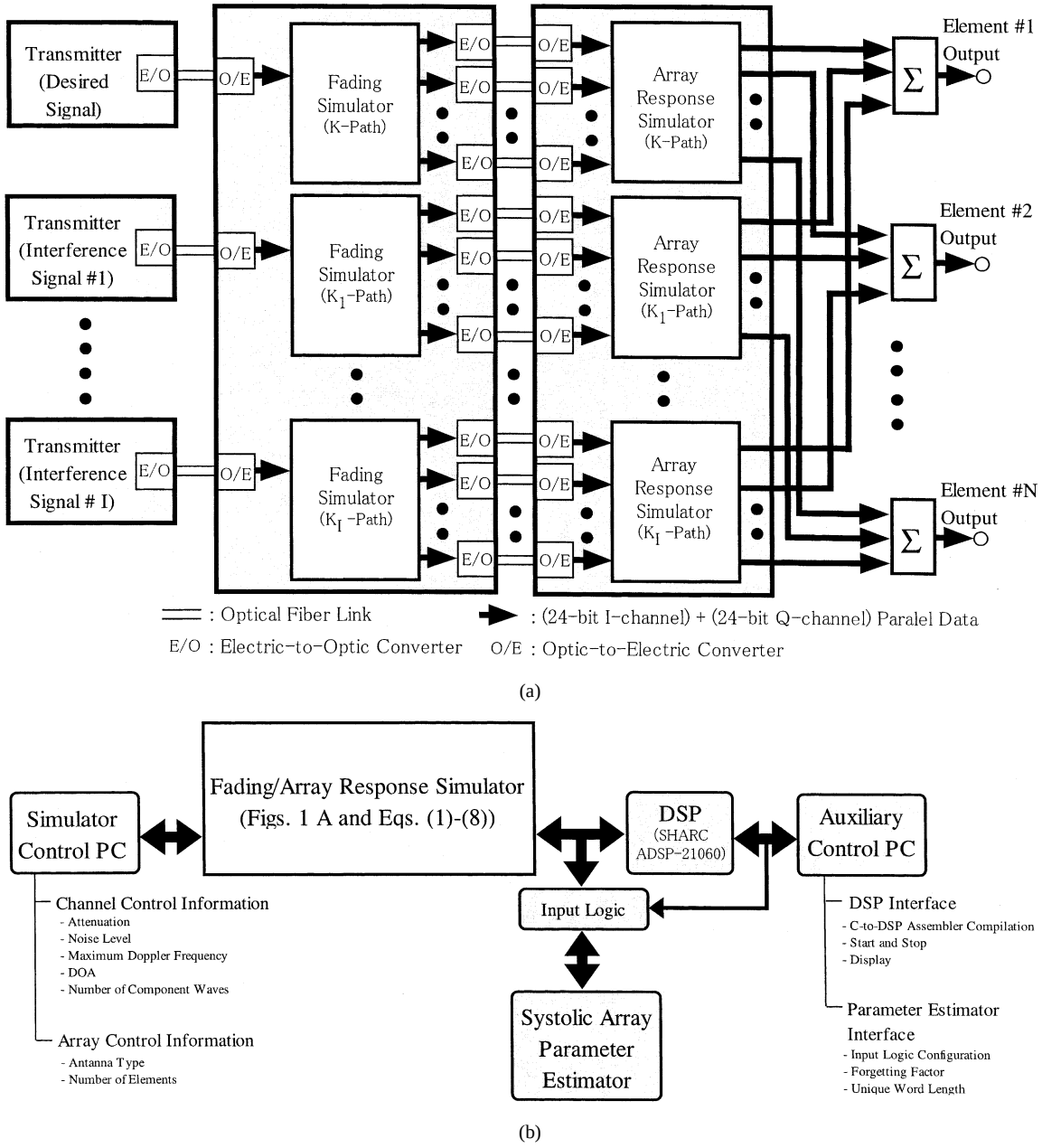


Fig. 1. (a) Block diagram of fading/array response simulator. (b) Control system and DSP/parameter estimator interface.

The primary purpose of this work is to provide a platform for experiments that will be conducted to evaluate the performance of the baseband sections of S/T-equalizers. This paper is organized as follows: Section II shows the channel model used in this paper, and provides mathematical expressions for each component of the model. Section III details the specifications of the developed simulation platform. Section IV presents results of the experiments conducted to verify the proper operation of the fading/array response simulator designed as a core part of the platform. Section V outlines an MMSE adaptive array [8] experiment using the DSP board of the platform. Some performance data obtained as a result of the experiments using the developed systems are then presented. Section V also describes results of an S/T-equalization experiment using the parameter estimation board of the platform.

II. Channel Model

Fig. 1(a) shows a block diagram of the fading/array response simulator developed as a core part of the platform. One desired and I interference users share the same channel. Signals transmitted from the $I+1$ mobile users are received by an N-element antenna array. A complex baseband expression of the N-dimensional vector channel is given by [4], [5]

$$\mathbf{x}(t) = \mathbf{h}(t) + \mathbf{g}(t) \tag{1}$$

where

$$\mathbf{h}(t) = \sum_{k=1}^{K} z_k(t) D(t - \tau_k) \mathbf{a}(\theta_k) + \sum_{i=1}^{I} \sum_{k'=1}^{K_i} z_{ik'}(t) U_i(t - \tau_{ik'}) \mathbf{a}(\theta_{ik'}) \tag{2}$$

is the antenna array output vector in the absence of noise. K and K_i are the number of the propagation paths with, respectively, the desired and the ith interference user, with

$$K_0 = K + \sum_{i=1}^{I} K_i \tag{3}$$

being the total number of the path components arriving at the base station.

$D(t)$ and $U_i(t)$ are, respectively, the desired user's and ith interferer's transmitted baseband signals. $z_k(t)$ and $z_{ik'}(t)$ are the fading complex envelopes with the desired user's kth path and the ith interferer's k'th path components, respectively, and τ_k and $\tau_{ik'}$ are the delays of these path components. $\mathbf{g}(t)$ is a filtered additive Gaussian noise vector. Each of the path components is associated with its DOA θ: using subscript k, θ_k denotes the DOA of the desired user's kth path, with ik', $\theta_{ik'}$ being the DOA of the ith interferer's k'th path. $\mathbf{a}(\theta_k)$ and $\mathbf{a}(\theta_{ik'})$ are the array responses for them.

In general, $\mathbf{a}(\theta)$ depends on the array geometry. For a linear array with element spacing L, $\mathbf{a}(\theta)$ becomes

$$\mathbf{a}(\theta) = \left[1, \exp\left\{j\,\frac{2\pi L}{\lambda}\sin\theta\right\}, \ldots, \exp\left\{j\,\frac{2\pi(N-1)L}{\lambda}\sin\theta\right\}\right]^t \tag{4}$$

where λ is the wave length of the carrier frequency. For a circular array with a minimum element spacing L,

$$\mathbf{a}(\theta) = \exp\left(-j\,\frac{\pi L}{\lambda\sin\left(\frac{\pi}{N}\right)}\right) \cdot \left[\cos\theta, \cos\left(\theta - \frac{2\pi}{N}\right), \ldots, \cos\left(\theta - \frac{2(N-1)\pi}{N}\right)\right]^t \tag{5}$$

Hence, simulating the array response $\mathbf{a}(\theta)$ imposed upon the received path component is equivalent to rotating its phases element-by-element, which is, in the complex baseband domain, further equivalent to multiplying the received signal by complex vector $\mathbf{a}(\theta)$.

Each path itself suffers from fading variations, which are, however, assumed to be frequency nonselective. One of the acceptable models of fading variation is the Jakes model, according to which the fading complex envelope $z(t)$ can be expressed as [9]

$$z(t) = \sum_{m=1}^{M} c_m \exp\{j(2\pi f_m t + \psi_m)\} \tag{6}$$

where $c_m \exp\{j(2\pi f_m t + \psi_m)\}$ is the mth component wave with c_m, f_m, and ψ_m being its normalized amplitude, frequency, and phase, respectively, and M is the number of component waves. The mobile's movement imposes a Doppler shift upon each of the component waves depending on their incident angles Θ_m as given by

$$f_m = f_D \cos\Theta_m \tag{7}$$

where f_D is the maximum Doppler frequency. Assuming the model in which uniformly distributed component *waves are emitted from around the mobile station in up-link (or arrive at the mobile station in down-link*), c_m and Θ_m can be approximated as $c_m = 1$, and

$$\Theta_m = \Theta_0 + \frac{2\pi(m-1)}{M} \tag{8}$$

where Θ_0 is a constant. The fading variations can be made statistically independent by setting the initial phases ψ_m of the component waves to follow a uniform distribution over [0, 2π].

Discrete-time signal processing takes place in the fading/array response simulator. Ordering of the discrete signal processing is indexed by a timing index n with $t = nT$, where $1/T$ is the sampling frequency. K_0 fading complex envelopes are generated according to Eqs. (6)–(8). Each path component is multiplied by its corresponding fading complex envelope, and then attenuated according to its strength, for which path components are multiplied by real constants. The fading path component is received by an N-element antenna array.

The phase rotation on each of the N antenna elements depends on the array geometry and the path's DOA. The array geometry and DOA on each path are input to the system controller from a PC. For each of the K_0 path components, the controller then calculates the phase rotations on each of the N antenna elements, and the path's N components received by the N elements are multiplied by the calculated N complex constants corresponding to their phase rotations element-by-element.

Signal processing based on the phase rotation is performed on an element-by-element basis; the phase-rotated K_0 path components are added together, further added to complex white Gaussian noise samples, and then filtered corresponding to the receiver filters assumed. N statistically independent two-dimensional random numbers uniformly distributed over [0, 1] are generated, and converted into N complex white Gaussian noise samples by using a look-up table following the Box–Muller method.

III. Specifications

This section describes detailed specifications of the developed simulation platform.

A. Fading/Array Response Simulator

1) Hardware: Table I summarizes the hardware specifications of the fading/array response simulator. 24-bit fixed point signal processing takes place corresponding to (1)–(3); in-phase and quadrature components of signals are expressed in a 24-bit data format. It ensures 16-bit accuracy at the output of the simulator, even in the presence of round-off due to the fixed-point signal processing.

The simulator performs signal processing at 24 Msamples/s, which indicates that if S samples are taken per symbol, a 24/S Msymbols/s signal can be transmitted. Symbol timing on the K_0 paths can be adjusted with 24 Msamples/s accuracy; if a 24-Msymbols/s signal is transmitted, all K_0 transmitted signals are assumed to be synchronized symbol-by-symbol. The flexible gate array (FPGA) is the main component of the simulator: most of the 24-bit fixed point 24 Msamples/s signal processing takes place in FPGAs. In many cases, transmitted data has to be formatted to meet the requirements of the experiment, to which

TABLE I
MAJOR SPECIFICATIONS OF FADING/ARRAY RESPONSE SIMULATOR

Item	Specifications
Signal Representation	Complex Baseband Domain (I/Q Vector Channel)
Data Format	24-bit Fixed Point/ Parallel Data
Sampling Speed	24 Msamples/sec
Number of Users	2
Number of Paths	2 for Each User, or 3 for Desired and 1 for Interferer
Delay Time	5.2 μsec Maximum (42nsec Step)
Doppler Frequency	2000 Hz Maximum
Number of Array Elements	8
Array Geometry	Linear and Circular

end framing can be realized flexibly by programming the FPGA device.

The key concepts of the simulator design are that the simulator components corresponding to the real network components, which are spatially separated in the real world, are implemented on physically separated hardware units, and that the network topology in terms of signal flow is simulated by simply connecting cables. For this purpose, as shown in Fig. 1(a), simulators of the transmitter and the multiple propagation paths with the desired user, those with the interference user, and the array response simulator were implemented as separate hardware units. However, it is quite difficult to synchronize all units at the 24 Msamples/s clock speed if the separated components are connected by 48-bit (=24-bit I-channel + 24-bit Q-channel) parallel cables.

To provide acceptable synchronization accuracy for 24 Msamples/s digital signal processing, the 48-bit data are parallel-to-serial converted and transmitted via optical fiber cables connecting the separated components. Sampling and unique word timings are multiplexed onto the serial data, and transmitted via the optical fiber cable. The total bit rate of the bit stream transmitted over the optical fiber cable is approximately 1.2 Gb/s (=$(48 + 2)$ bits $\times$ 24 Msamples/s + *overhead for the optical fiber link*). The transmitted 48-bit parallel data, and the sampling and unique word timings are then recovered by a serial-to-parallel conversion at the receiver component side. The sampling and unique words timing extracted from the received serial data provide the receiver component with clock and frame timing, respectively. This corresponds to the real world situation wherein the clock and frame timing are recovered perfectly at the receiver side.

2) Software: As shown in Fig. 1(b), two PCs are connected to the simulator; one controls the simulator while the other, the auxiliary control PC, controls the DSP and the systolic array parameter estimator. Channel control information and array control information are provided by the simulator control PC. The channel control information includes:

1) attenuation on each path;
2) noise level on each antenna element;
3) maximum Doppler frequency f_D for each of the desired and interference users;
4) DOA of each path;
5) number of component waves related to fading variation on each path.

The array control information includes:

1) antenna type;
2) number of antenna elements;

both of which are associated with the array geometry. The channel control information and the array control information are sent to the simulator via an RS232c interface.

The array response $\mathbf{a}(\theta_k)$, $1 \leq k \leq K_0$, corresponding to the path's DOA θ_k is calculated, and the N values of $\mathbf{a}(\theta_k)$'s elements are set as the complex coefficients to be multiplied by the received signal components at their corresponding antenna elements. The simulator can support N-element linear and circular arrays if their minimum element spacing is half the wavelength.

The auxiliary control PC is used as an operation platform for the DSP and the parameter estimator. The PC has the following capabilities:

1) C-to-DSP Assembler compilation;
2) Start-and-Stop the program on the DSP;
3) configure the systolic array input logic;
4) input forgetting factor and unique word length to the parameter estimator;
5) display the algorithm output.

The DSP and the parameter estimator are interfaced to the simulator hardware. A series of array output vectors is used in the programs used to realize the algorithms in real-time. The algorithm output can yield the beam patterns that indicate antenna directivity and/or some performance characteristics such as bit error rate (BER), both of which are displayed on the PC screen.

B. Parameter Estimator

The parameter estimation algorithms required in S/T-equalization problems may be run using DSP chips, but complexity sometimes exceed the practical limit of the DSP's computation power at high transmission bit rates. To overcome this problem, several pipelining techniques for hardware implementation of the RLS algorithm, which are commonly referred to as systolic array techniques, have been proposed [7], [10]–[13]. We have developed an ASIC chip set for a systolic array implementation of the RLS algorithm [6]. 32-bit fixed point signal processing takes place in the processor; one cycle of internal cell signal processing requires about 500 ns, and boundary cell signal processing about 80 ns. More details about the chip set are given in [6].

A parameter estimator board was developed using the chip set with the aim of applying it in the simulation platform. The board can estimate up to 23 parameters and supports the estimation of arbitrary combinations of spatial and temporal parameters. The parameter estimation process, which can be triggered by the

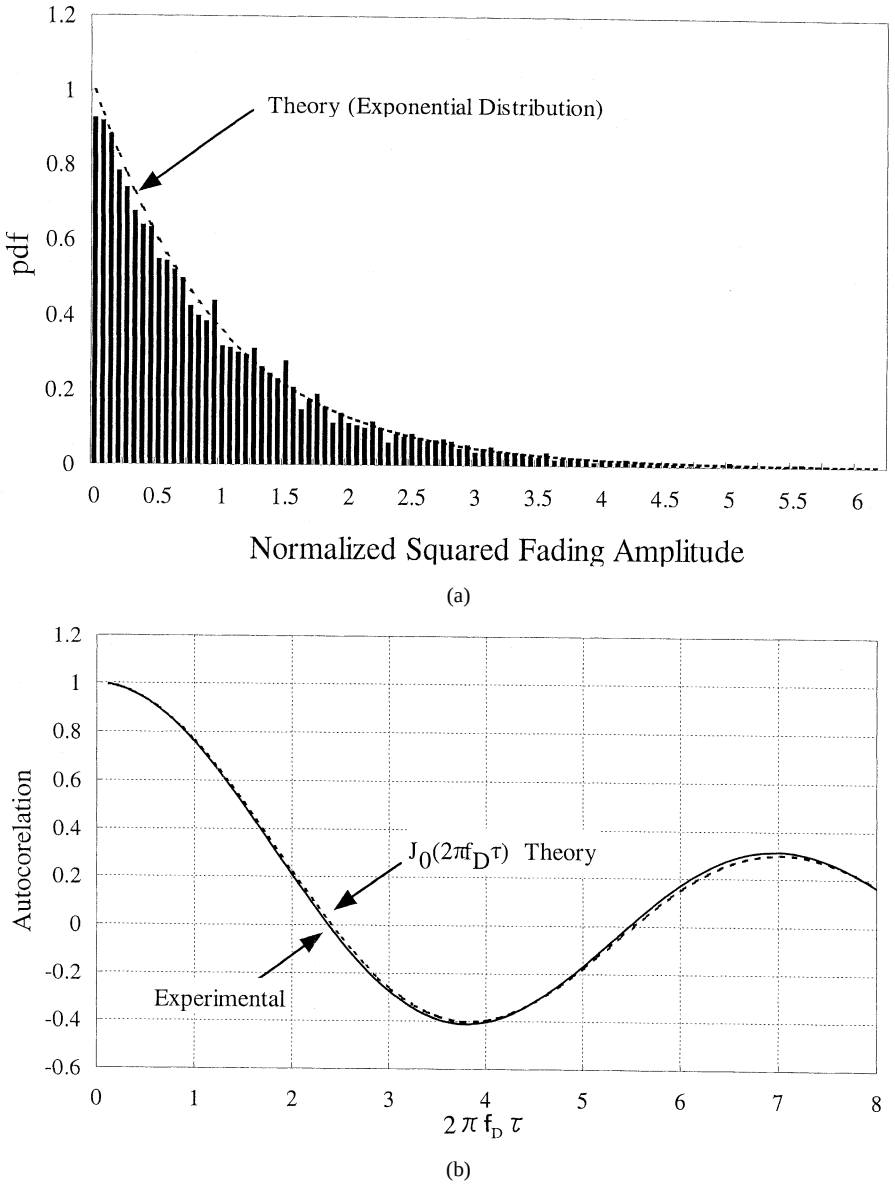


Fig. 2. (a) pdf of normalized squared fading amplitude. (b) Autocorrelation function of fading complex envelope.

DSP, takes place while the DSP is running programs for other purposes such as sequence estimation.

IV. Component Performance

This Section presents results of the experiments conducted to verify the proper operation of the fading/array response simulator. Fig. 2(a) and (b) shows two basic characteristics of the simulated fading: Fig. 2(a) shows a sample probability density function $p(|z_k(t)|^2)$ of squared fading amplitude $|z_k(t)|^2$; Fig. 2(b) a sample autocorrelation function $\rho(\tau)$ of fading complex envelope $z_k(t)$. With the multipath fading model described in Section II, $\langle |z(t)|^2 \rangle = 1$, $p(|z(t)|^2) = \exp(-|z(t)|^2)$, and $\rho(\tau) = J_0(2\pi f_D \tau)$; all of these relationships hold independently of path number k, so index k has been eliminated. The theoretical curves of the probability density and autocorrelation functions are also plotted in Fig. 2(a) and (b). The sample functions are quite consistent with the theoretical curves.

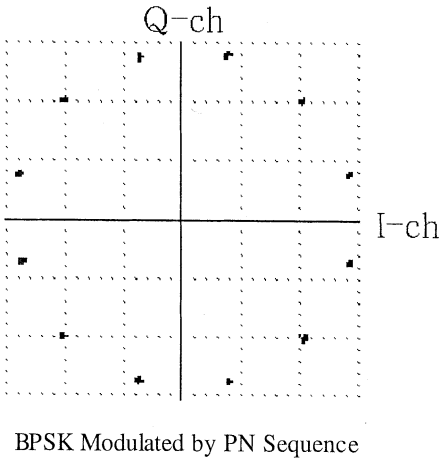
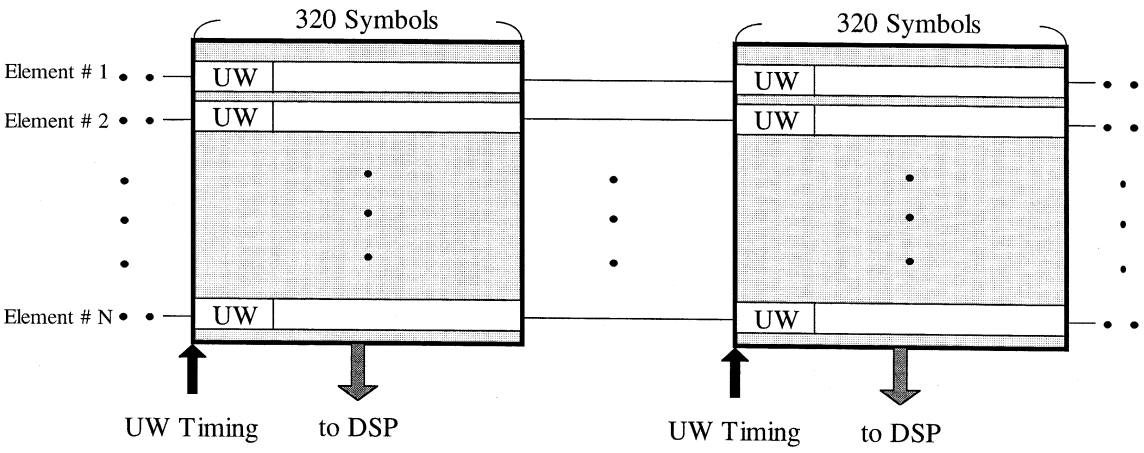


Fig. 3. Rotated received signal points at the output of an array antenna element.

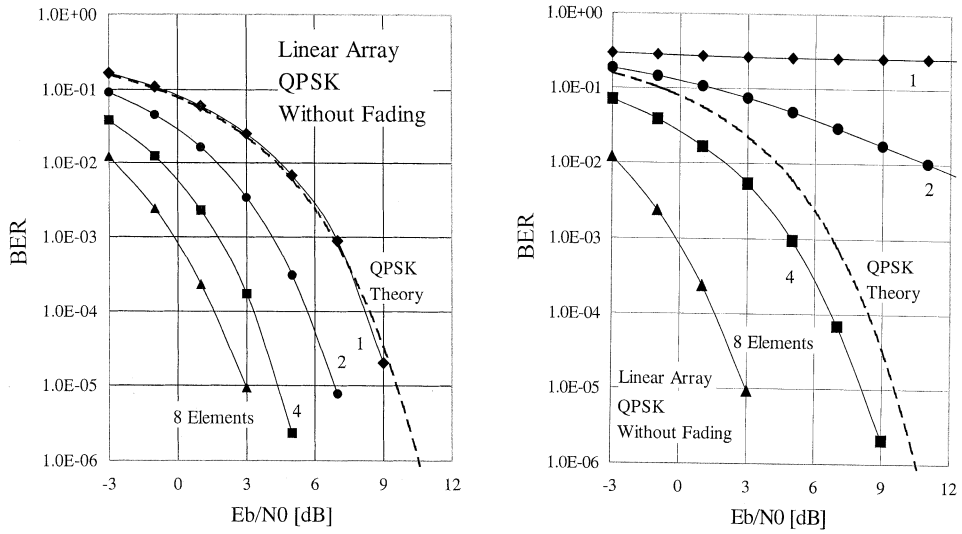
Fig. 3 shows, in the complex baseband domain, the received signal points rotated by complex constants corresponding to the

TABLE II
EXPERIMENT CONDITIONS

Modulation Scheme		QPSK
Baud Rate		6 Msymbols/sec
Frame Length		320 Symbols
Array Geometry		Linear Array with λ/2 Elemet Spacing
MMSE Adaptive Array	Effective Symbol Rate	Approx. 2.2 ksymbols/sec
	Training Length	31 Symbols
	Algorithm	MMSE/RLS
	Forgetting Factor	0.9
	Number of Elements	1～8



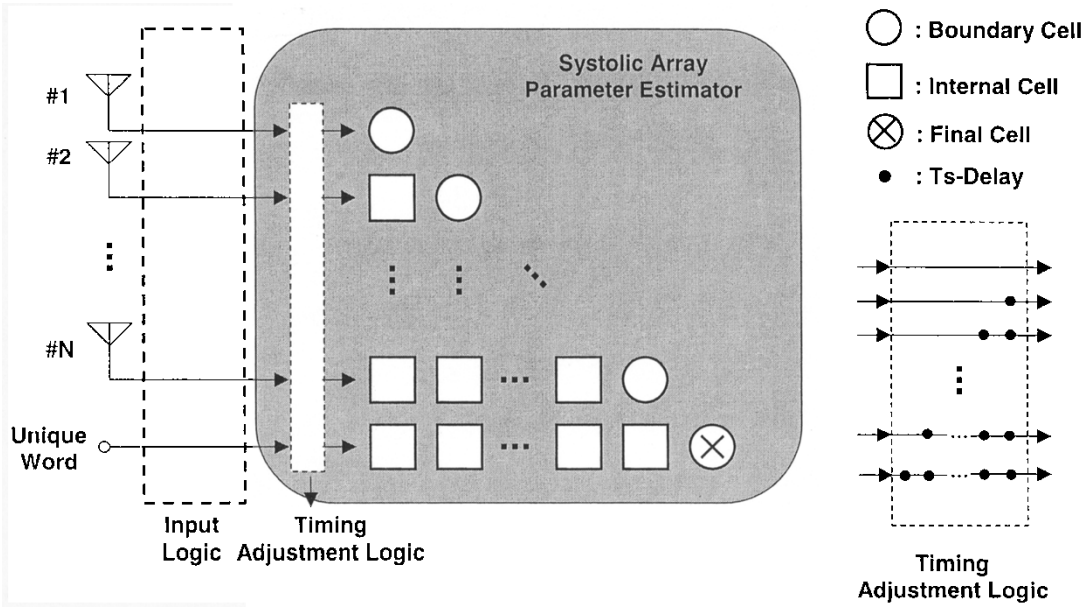
(a)



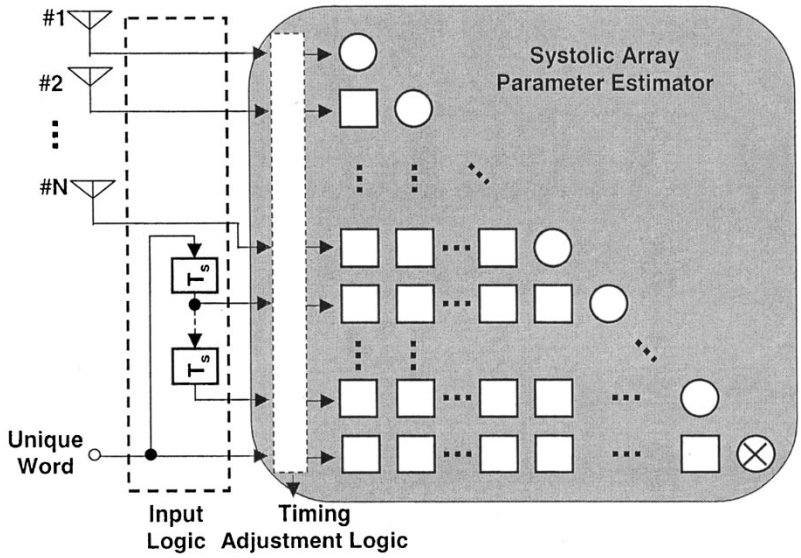
(b) (c)

Fig. 4. (a) Data flow for signal reception in the experiments. (b) MMSE adaptive array BER performance without interference: DOA with received signal of 20°. (c) MMSE adaptive array BER performance with interference: DOA with desired signal of 20°, and DOAs with interference sources at 40 and 60°.

phase rotations at an array antenna element, where a binary phase shift-keyed (BPSK) signal modulated by a pseudo random (PN) sequence was transmitted and no fading was assumed. Complex constants $\exp\{j(\pi/6+k\pi/4)\}$s with $0 \leq k \leq 5$ were



(a)



(b)

Fig. 5. (a) Input logic configurations for S/T-equalizers without time-domain taps. (b) Input logic configurations for S/T-equalizers with time-domain taps.

multiplied by the received signal having no phase rotation, resulting in the signal points indicated in Fig. 3.

V. System Performance

A. MMSE Adaptive Array Simulation

A DSP program for an MMSE adaptive array algorithm was developed. The program was then run to check its proper operability on the channel platform (the systolic array parameter estimator was not used in this experiment). Table II summarizes the conditions assumed in the experiments. Quaternary PSK (QPSK) was assumed as the modulation scheme. Each frame was 320 symbols long, consisting of included 31 symbols unique word and 289 symbol information sequences. Three path components arrived at the receiver: one is the desired while the others are the interference and its one symbol-delayed path components. The desired signal's DOA was 20°, and the two interference components' DOAs were 40° and 60°. An N-element linear array with a minimum element spacing of half the wavelength was assumed.

To adjust the DSP's signal processing capability to the simulator's 24 Msamples/s sampling speed, received frames, each consisting of $320 \times N$ signal samples, were periodically input to the DSP. Fig. 4(a) shows a timing chart for signal reception. The effective symbol rate with the DSP-based MMSE adaptive array signal processing was about 2 ksymbol/s. The receiver has a knowledge about the unique word waveform and its timing, and the adaptive array algorithm uses them as the desired response and timing reference, respectively. The tap weights were updated by using the RLS algorithm.

Fig. 4(b) and (c) show measured BER performance with the number of the antenna elements, N, as a parameter: Fig. 4(b) is

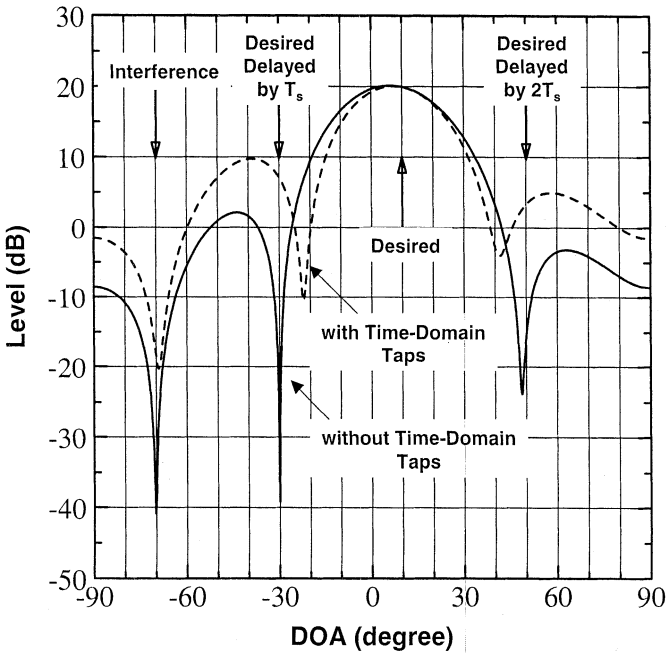


Fig. 6. Beam patterns with two types of S/T-equalizers: Dashed/solid lines for with/without time-domain taps.

without interference, while Fig. 4(c) has two interference users. Fading was absent in both cases. The asymptotic gain is defined as the reduction in the ratio of the per-bit signal energy to the noise power spectral density (E_b/N_0) compared to QPSK coherent detection with large E_b/N_0. It is obvious that without interference the theoretical asymptotic gain is $10\log_{10} N$ in dB. It is found from Fig. 4(b) that the experimental performance curves with $1 \leq N \leq 4$ well support the asymptotic gains. With $N = 8$, the gain is slightly smaller than the theoretical one. This is because mainly the RLS algorithm fails to determine the optimum tap weights. Adjusting the values of the RLS-related parameters such as the forgetting factor as well as the initial conditions of the algorithm should improve performance, however, such optimization details exceed the scope of this paper.

In the presence of interference, the number of antenna elements, N, determines the maximum number of interference sources that can be suppressed. Since, in Fig. 4(c)'s case, there are two interferers, both having the same strength as the desired signal, they can be suppressed if $N \geq 3$ as can be observed in Fig. 4(c). In the presence of interference, the asymptotic gain depends on the DOAs of the incident signal components. If the DOAs of the desired and two interference signals are 20°, 40°, and 60°, respectively, the gains are 1.5 dB with $N = 4$ and 8.9 dB with $N = 8$. With $N = 4$, the 1.5 dB gain is well supported by its corresponding experimental curve in Fig. 4(c), but with $N = 8$ the gain value of 8.9 dB can not be reached for the same reason given in the without interference case.

B. S/T-Equalizer Using Parameter Estimator Simulation

When the systolic array board is used for parameter estimation as a part of the algorithm to be evaluated using the platform, data input logic has to be configured to match the type of S/T-equalizer. Fig. 5 shows input logic configurations for two types of S/T-equalizers: Fig. 5(a) is for the case where one interference and two delayed desired signal components should be nullified; Fig. 5(b) for the case where only interference components to be nullified (Delayed desired components can be combined somehow by a time-domain equalizer following the adaptive array. Detailed investigations on the S/T-equalization algorithm [14] used in the simulations exceed the scope of this paper. The algorithm details and performance curves can be seen in Ref. [14].) Fig. 6 shows for the element number $N = 4$ and received $E_b/N_0 = 20$ dB the beam patterns obtained from the parameter estimation using the systolic array board for the two cases: the solid line is for Fig. 5(a)'s configuration; the dashed line for Fig. 5(b)'s. It is found that with Fig. 5(a)'s configuration, nulls are formed toward the interference and delayed desired components, while with Fig. 5(b)'s, nulls are not formed toward delayed desired signal components. This leaves the possibility that the delayed desired signal components are combined to achieve diversity improvement by time-domain signal processing for sequence estimation.

VI. Conclusion

This paper has outlined a complex baseband platform developed for spatial–temporal mobile radio channel simulations. The platform consists of a complex baseband fading/array response simulator, a DSP (Analog Devices SHARC ADSP-21 060) board, and a general-purpose parameter estimator that uses systolic array implementation of the RLS algorithm. The developed simulation platform operates completely in the complex baseband domain. The fading/array response simulator replicates temporal and spatial radio wave propagation scenarios in broadband mobile communication channels. Up to 23 parameters can be estimated by using the systolic array parameter estimator, whose capability supports the testing of arbitrary combinations of spatial and temporal parameters. The parameter estimation process, which can be triggered by the DSP, takes place while the DSP is running programs for other purposes such as sequence estimation.

Proper operation of the developed platform was verified through a series of experiments. The correct operation of the fading/array response simulator's key components were first evaluated such as probability density and autocorrelation functions of the generated fading complex envelope as well as the phase rotations imposed upon received signal components at each of the antenna elements. Overall system performance was then evaluated through experiments using the DSP board running an MMSE adaptive array algorithm. An S/T-equalizer having taps in both the spatial and temporal domains was also simulated using the DSP board and systolic array parameter estimator. It has been shown that data obtained in the experiments are reasonable and satisfactory, which confirms that the developed simulation platform operates as intended.

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