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Description	

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Fabrication of GaAs MISFET With nm-Thin Oxidized Layer Formed by UV and Ozone Process

Koichi Iiyama, *Member, IEEE*, Yukihiro Kita, Yosuke Ohta, Masaaki Nasuno, Saburo Takamiya, Koichi Higashimine, and Nobuo Ohtsuka

***Abstract*—A gate insulating layer with single nm-order thickness for suppressing gate leakage current is one of the key factors in extending downsizing limits, based upon the scaling rule, of field-effect-type transistors. We describe the fabrication and characterization of GaAs MISFETs with a nm-thin oxidized layer as the gate insulating layer, which is formed by an ultraviolet (UV) and ozone process. The UV and ozone process forms oxidized GaAs layers near the surface, which effectively suppress the reverse leakage current by several orders of magnitude. The fabricated GaAs MISFET can operate not only in the depletion mode, but also in the accumulation mode up to 3 V of the gate voltage for 8-nm-thick oxidized layer due to the current blocking effect of the oxidized layer. A current cutoff frequency of 6 GHz and a maximum oscillation frequency of 8 GHz are obtained for a GaAs MISFET with a 1-μm-long gate length and 8-nm-thick oxidized layer.**

***Index Terms*—Compound semiconductors, GaAs, MISFET, self-align, ultraviolet (UV) and ozone process.**

I. Introduction

COMPOUND semiconductor field effect transistors (FETs) and high-electron mobility transistors (HEMTs) are widely used in mobile telephones and high-speed optoelectronic circuits, such as optical receivers, and are very promising electronic devices in high-speed optical communication systems over 40 Gb/s, satellite communication systems, intelligent transport systems (ITS) etc. In the compound semiconductor FETs and HEMTs, Schottky junction has been used as the gate structure for a long time, and a cutoff frequency of $f_T = 396$ GHz was obtained in 2001 [1]. However, the progress in the cutoff frequency is very slow (from $f_T = 342$ GHz [2] in 1992 to 396 GHz in 2001) because of short-channel effects (SCEs). In the Schottky gate structure, the gate leakage current increases due to tunneling effect according to an increase of the donor density which accompanies with downsizing the device to achieve high-speed operation.

The alternative gate structure is the metal-insulator-semiconductor (MIS) to reduce the gate leakage current and to overcome the SCE [3], [4]. The advantages of the MIS gate structure are as follows:

1) high-speed operation due to downsizing the device more and more;
2) possibility of single power supply due to enhancement mode operation;
3) possibility of complementary device structure;
4) improvement of thermal property and breakdown voltage.

However, no MIS-gate FET/HEMT has been practically used because a high-quality thin-film insulating layer cannot be achieved on the surface of the compound semiconductor due to high density of interface states. A number of MIS gate structures have been tried for realizing MISFET to date. The insulated gate InGaAs/InAlAs PHEMT utilizing a silicon interface control layer was reported [4]. The *in-situ* Ga_2O_3/Gd_2O_3 film growth on GaAs by molecular beam epitaxy (MBE) was reported for GaAs MISFET [5]. The GaAs MISFET with SiO_2 as the insulating layer [6] and the GaAs MOSFET with oxidized GaAs as the insulating layer [7] were also reported. These reports show some good results for high-performance GaAs MISFETs. However, the thickness of the insulating layers in such GaAs MISFETs are relatively thick (20 nm–40 nm). To achieve ultra-high-speed transistor which can operate in a terahertz frequency range, a nm-thin insulating layer is necessary.

We have been studying the MIS gate structure with a nm-thin GaAs-oxide layer prepared by ultraviolet (UV) and ozone treatment [8]. The gate leakage current can be suppressed by five orders of magnitude with an 8-nm-thin GaAs-oxidized layer. In this paper, we present GaAs MISFETs with nm-thin GaAs-oxide layers formed by a UV and ozone process including microscopic structural details and RF performance in addition to our previous work [9], focusing on the gate current suppression effect.

II. UV and Ozone Process

The oxidation of the GaAs surface was carried out by UV and ozone process (SAMCO: UV and Ozone Cleaner, UV-1). After removing the native oxide layer on the surface of *n*-GaAs/semi-insulating-GaAs wafers by buffered hydrofluoric acid, the wafers were directly oxidized by the UV and ozone process for $15 \sim 480$ min at the wafer stage temeperature of 300 °C. Then, the oxidized layer was partially removed photolithographically by buffered hydrofluoric acid etching, and the thickness was measured by using an atomic force microscope (AFM). The measured thickness of the oxidized layer against the UV and ozone time is shown in Fig. 1. The oxidation at 100 °C for 240 min was also carried out, which resulted in the oxide thickness of $6 \sim 9$ nm, suggesting very

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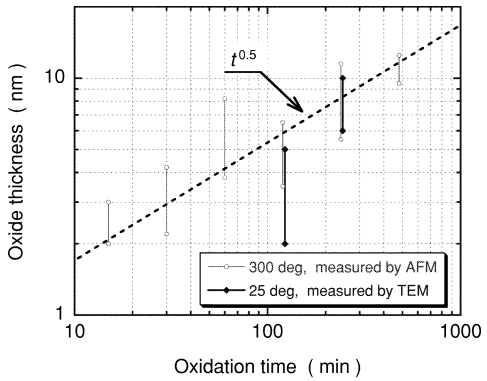

Fig. 1. Measured thickness of the oxidized layer against the UV and ozone time.

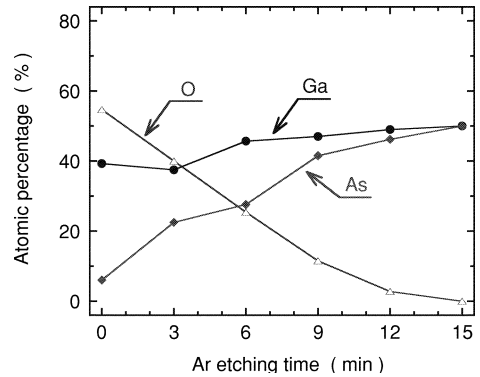

Fig. 2. Measured composition of the oxidized layer by the XPS.

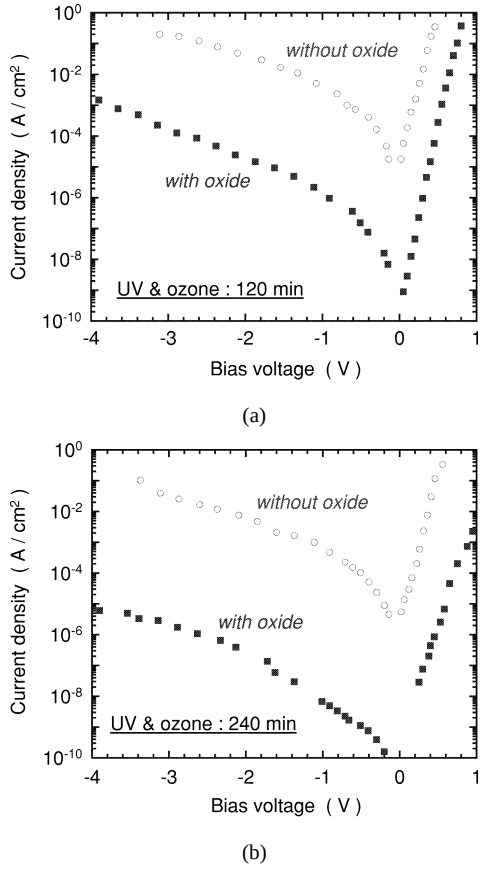

Fig. 3. Measured $I-V$ characteristics for both the Schottky and the MIS diodes. (a) UV and ozone time: 120 min. (b) UV and ozone time: 240 min.

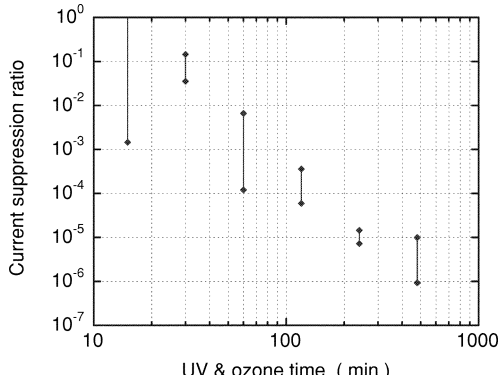

Fig. 4. Current suppression ratio of the MIS diode to the current of the Schottky diode.

weak dependence on the temperature. The uncertain range for each data indicates positional dependence of the measured data, reflecting the nonuniformity of the thickness of the oxidized layer. The thickness is nearly proportional to square root of the oxidation time. The thickness of the oxidized layer processed at 25 °C is also shown in Fig. 1, which was measured by the cross-sectional high-resolution transmission electron microscope (TEM), as described in Section III. No significant dependency of the thickness of the oxidized layer on the oxidation temperature is observed.

X-ray photoelectron spectroscopy (XPS) analysis was carried out to investigate the composition of the oxidized layer. Fig. 2 shows the measured composition of a 480-min oxidized surface against the Ar etching time that reflects the depth. Fig. 2 suggests the outdiffusion and the decomposition of As near the surface and the incorporation of oxygen. Due to insufficient depth resolution ($\approx$ 10 nm) of the XPS, Fig. 2 does not show accurate distributions. However, it clearly suggests that the oxide layer is mainly composed of Ga-oxide (mainly Ga_2O_3), although As-oxide (As_2O_3, As_2O_5) may still remain to some extent.

Next, we measured the *I–V* characteristics for both the Schottky diodes and the MIS diodes. Fig. 3 shows the measured results for the Schottky (open circles) and the MIS diodes (closed circles). It can clearly be seen that the nm-thin insulating layers effectively suppress the reverse leakage currents while keeping the shapes of the curves. Fig. 4 shows the current suppression ratio of the MIS diode to the current of the Schottky diode. The current can be suppressed by five orders of magnitude when the oxidation was carried out for 240 min.

III. Device Structure and Fabrication

The structure of the fabricated GaAs MISFET is shown in Fig. 5. The substrate used in our experiments was *n*-GaAs (donor concentration: 3.1×10^{17} cm^{-3}, thickness: 0.42 μm)/semi-insulating-GaAs epitaxial wafer. The native oxide layer on the surface of the substrate was first removed by buffered hydrofluoric acid etching and the epitaxial layer was thinned to 0.29 μm by etching in order to reduce the mesa-step-height, then rinsed by deionized water. The drain and

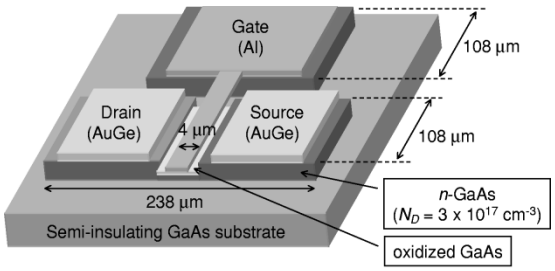

Fig. 5. Structure of the fabricated GaAs MISFET.

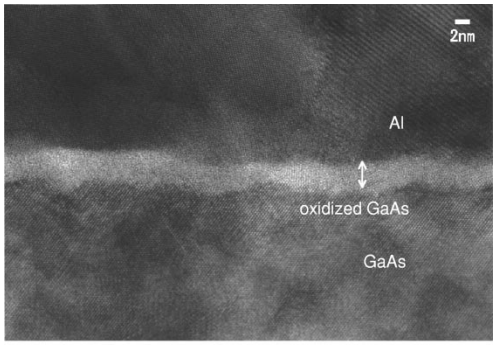

Fig. 6. Cross-sectional high-resolution TEM image of the thin oxide layer existing between the GaAs and the Al gate electrode. The magnification is 3 750 000.

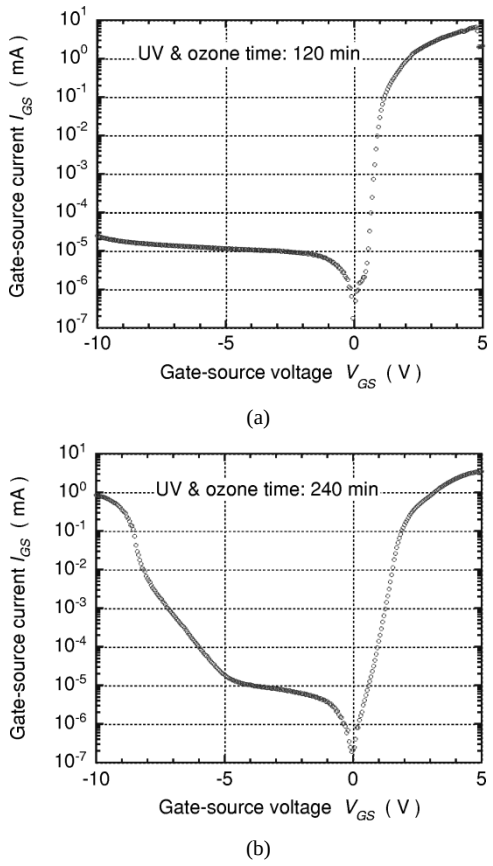

Fig. 7. $I-V$ characteristics between the gate and the source for the GaAs MISFET with the UV and ozone times of 120 min and 240 min. (a) UV and ozone time: 120 min. (b) UV and ozone time: 240 min.

the source electrodes were formed by evaporating AuGe and then sintered at 367 °C for 1 min. After mesa-etching the epitaxial layer by the etchant ($H_3PO_4 : H_2O : H_2O_2 = 4 : 90 : 1$) for isolating the gate, a photoresist was coated and patterned for the recess etching, the oxidation of the GaAs, and the formation of the gate electrode with a self-align process. The recess etching was carried out by using the same etchant, and a typical resultant recess thickness was 0.16 μm. Then, the sample was oxidized by the UV and ozone process at room temperature. Only the recess region was selectively oxidized by the presence of the photoresist mask pattern. Then, Al was deposited for the gate electrode, and finally the photoresist mask pattern was removed. The gate length and the gate width were 4 μm and 100 μm, respectively.

Fig. 6 shows the cross-sectional high-resolution TEM image of the thin oxidized layer existing between the GaAs and the Al gate electrode. The oxidation was carried out at 25 °C for 120 min. The image was taken in the (110) direction of the GaAs. The oxide layer appears as an amorphous image, while the GaAs and the Al exhibit lattice fringes. Periodic fringes are seen in some small regions in the oxide layer, which may be attributed to overlapping of the oxide layer with either the GaAs or the Al crystals in the imaging direction due to the wavy interfaces. Moire fringes are seen in the Al crystalline regions, which are caused by overlapping of different crystalline grains. Both the flatness of the interface between the GaAs and the oxidized layer and the thickness of the oxidized layer are far from atomic flat. The thickness of the oxide layer is position-dependent and can be read to be $2 \sim 5$ nm, which is plotted in Fig. 1. Similar TEM observation was also carried out for a 240-min oxidized sample, and the oxide thickness of $6 \sim 10$ nm was obtained.

IV. DC Characteristics

Fig. 7 shows the current–voltage (I–V) characteristics between the gate and the source for the GaAs MISFETs with the UV and ozone time of 120 min and 240 min. The device with the oxidation time of 240 min has smaller forward current due to current blocking effect by the oxidized GaAs layer. For the backward bias voltage larger than -5 V, the device with the oxidation time of 240 min has larger backward current. This may be due to the Fowler-Nordheim (FN) tunneling. In the MISFETs, the nm-order insulating layer and the depletion layer with several tens $\sim$ 100 nm thickness share the bias voltage. When the insulating layer is very thin and the tunneling prevents accumulation of holes at the interface between the GaAs and the oxidized GaAs, most of the bias voltage is applied to the depletion layer like a Schottky junction. When the insulating layer becomes thick enough to prevent the tunneling, an additional bias voltage is mostly applied to the oxidized layer and causes the FN tunneling. In the case of SiO_2/Si systems as a reference, the critical SiO_2 thickness is about 4 nm [10]. The thickness of the oxidized GaAs layers estimated by the TEM (see Fig. 1) are approximately 3 nm and 8 nm for the oxidation time of 120 min and 240 min, respectively. The thicker oxidized layer may accumulate holes at the insulator-semiconductor (IS) interface, and then the additional bias voltage is applied only to the oxidized layer, which causes the FN tunneling.

Fig. 8 shows the measured drain current-drain voltage (I_D–V_D) characteristics for the GaAs MISFETs along with

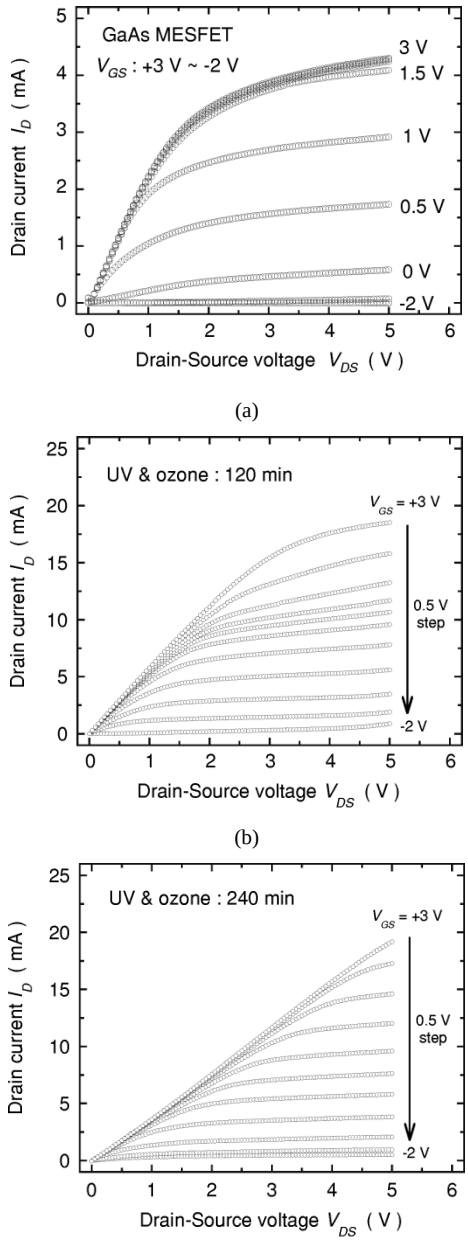

Fig. 8. Drain current-drain voltage (I_D–V_D) characteristics for the GaAs MEFET and GaAs MISFET with the UV and ozone times of 120 min and 240 min. The thickness of the oxide layers estimated by the TEM image are 3 nm and 8 nm, respectively. (a) GaAs MEFET. (b) UV and ozone time: 120 min. (c) UV and ozone time: 240 min.

that for the MESFET by using a semiconductor parameter analyzer (Hewlett Packard: HP 4156A). The UV and ozone process was 120 min and 240 min at room temperature. The thickness of the oxidized layer was estimated to be 3 nm and 8 nm, respectively, from the TEM image. The gate voltage was changed from -2 V to $+3$ V with 0.5 V step. In the GaAs MESFET [see Fig. 8(a)], the drain current is saturated when the gate voltage reaches $+1.5$ V. However, in the GaAs MISFETs, the drain current increases until the gate voltage reaches $+3$ V. Thus, the MISFETs can operate even under accumulation mode (beyond the flat-band condition) in spite of such ultrathin insulating layers. This result coincides well with the gate voltage which gives mA-order forward gate current (see Fig. 7), and means that the injected electrons from the source is directed to the drain without leaking to the gate due to current blocking by the oxidized nm-thin GaAs layer. A high ohmic contact resistance also increases the saturation gate voltage. However, Fig. 7 clearly shows that the forward voltage at a certain current increases with the oxide thickness even below the series-resistance-limited current region, verifying the current blocking effect of the insulating layer. The difference of the drain current between the MESFET and the MISFETs is mainly due to the difference of the recess thickness from wafer to wafer. We also find out that the transconductance decreases when the gate voltage is around the flat-band voltage ($+0.5$ V $\sim$ $+1.5$ V) for the device with the UV and ozone time of 120 min. Most of the samples with 120 min oxidation and some of the samples with 240 min oxidation show such recessed transcoductances around the flat-band voltage.

We also measured the I_D–V_D characteristics by using an analog semiconductor curve tracer (Iwatsu: TT-507). The I_D–V_D characteristics have hysteresis loop, and a large hysteresis loop was observed when the gate voltage is around the flat-band voltage. This implies the existence of movable ion or trap/release mechanism of charges in the oxidized layer and/or the interface between the GaAs and the oxidized layer.

Fig. 9 shows the measured transconductance against the gate voltage. The transconductance drops around the flat-band voltage for the device with the UV and ozone time of 120 min. This may be caused by a combination of trap/release and spatial distributions of electrons, as described in Section VI. The maximum transconductance is $50 \sim 60$ mS/mm. Such a low transconductance is due to the long gate length and the nonoptimized recess etching.

Long-term reliability test of the MISFETs is not performed due to the remaining hysteresis problem. However, power consumption ($I_D \times V_{DS}$) at the device failure for the device with the oxdation time of 240 min, tested by the curve tracer, is nearly equal to that of a commercial low-noise GaAs MESFET with a nearly equal gate width.

V. RF Characteristics

We fabricated similar MISFET with a coplaner electrode structure and the AuGe/Ni source and drain electrodes, as shown in Fig. 10 for on-wafer measurement of S parameters of the device. The UV and ozone time was 240 min, and the gate length and the gate width are 1 μm and 80 μm (40 μm$\times$ 2 fingers), respectively. Fig. 11(a) shows the measured I_D–V_D characteristic of the device (1 finger). Due to the small gate width and excess recess etching, the drain current is smaller than that shown in Fig. 7. However, the availability of the forward gate bias operation beyond the flat-band voltage and the recessed transconductance around the flat-band condition are reproduced. Fig. 11(b) shows the stability factor K, the maximum available power gain (MAG), the maximum stable power gain (MSG), and the $|h_{21}|^2$ evaluated from the measured S parameters. The drain and the gate voltages are $V_{DS} = +4$ V and $V_{GS} = +1$ V, respectively. The current cutoff frequency f_T and the maximum oscillation frequency $f_{\rm osc}$ are estimated to be $f_T = 6$ GHz and $f_{\rm osc} = 8$ GHz, respectively. We also

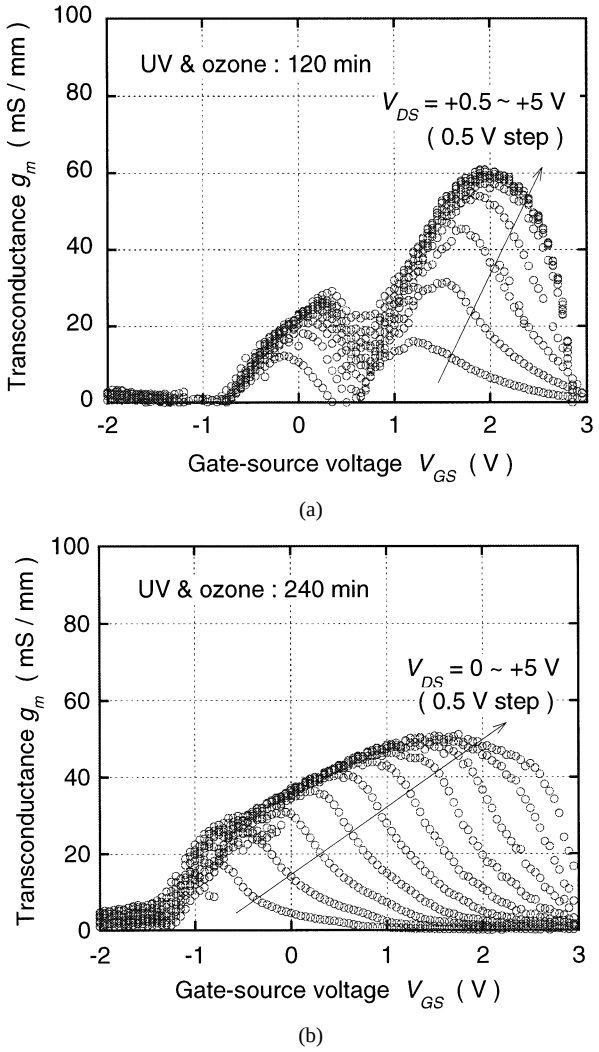

Fig. 9. Measured transconductance against the gate voltage of the GaAs MISFET with the UV and ozone times of 120 min and 240 min. (a) UV and ozone time: 120 min. (b) UV and ozone time: 240 min.

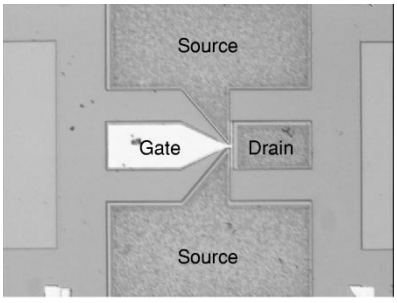

Fig. 10. Photograph of the fabricated GaAs MISFET with a coplaner electrode structure.

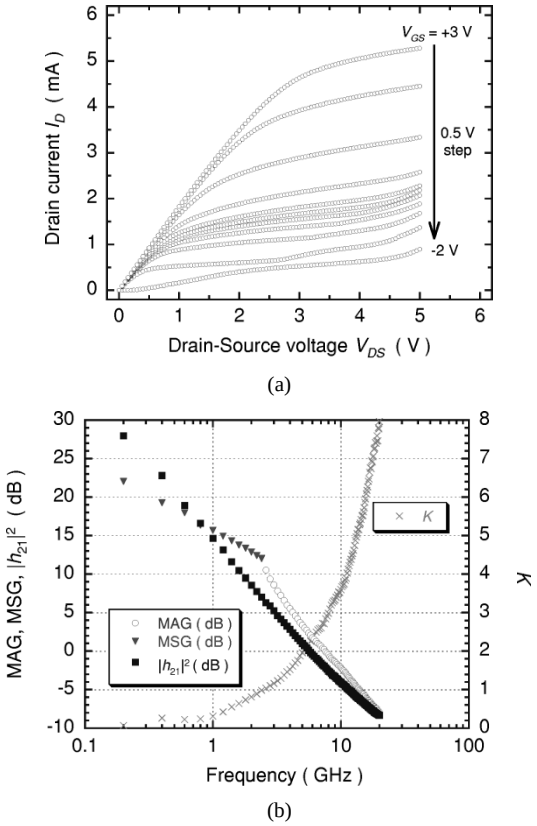

Fig. 11. Measured I_D–V_D characteristic and the RF characteristics of the GaAs MISFET. The UV and ozone time is 240 min, and the gate length and the gate width are 1 μm and 80 μm, respectively. $V_{DS} = +4$ V and $V_{GS} = +1$ V. (a) I_D–V_D characteristic. (b) RF characteristics.

measured the device at $V_{DS} = +4$ V and $V_{GS} = +2$ V, but no substantial change in the RF performance was observed. This implies that the recessed transconductance of the dc I_D–V_D curve does not directly affect the RF performance. The main reasons for the relatively low f_T and $f_{\max}$ are relatively high ohmic contact, estimated to be $R_{DS} = 600\,\Omega$ from Fig. 11(a), and an unoptimized recess thickness.

VI. Discussions

The nonuniform oxide thickness could be one of the problems which causes different performances between the devices even in a wafer, especially in the thinner oxide devices. Fig. 12 shows oxidation time-dependence of the roughness of the oxide surfaces and the oxide/GaAs interfaces. The surface roughness increases with increasing oxidation time, but the interface roughness decreases with increasing oxidation time. This trend is similar to that reported for thermally oxidized SiO_2/Si systems [11], and suggests that the interface inherently tends to approach a perfect (100) plane by long-time oxidation. Hence, the nonuniformity of the oxide thickness can be minimized by using (100) wafer with minimized surface roughness, which is obtainable by removing an oxide layer after long-time oxidation, using a combination of heteroepitaxial growth, material-selective etching, etc.

Most of the samples with the oxidation time of 120 min and some of the samples with the oxidation time of 240 min show a drop in the transconductances around the flat-band voltage. The main reason we attribute it to trap/release of electrons is as follows. We measured the leakage currents of Ni/*n*-GaAs Schottky junctions which were formed after UV and ozone oxidation and removal of the oxidated layers. They showed much larger leakage currents than the Schottky junction formed on an original GaAs surface [8]. This suggests that the oxidation process creates deep levels in the GaAs wafers near the IS interfaces. The leakage current increased with the oxidation time up to 120 min, and then decreased by longer oxidation time. Our

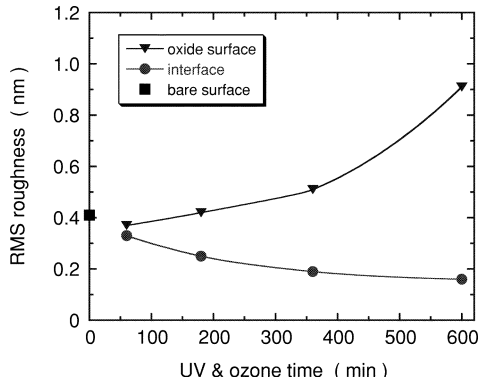

Fig. 12. Measured RMS roughness of the oxide layer and the interface against the oxidation time.

recent work [12], [13] on the *C–V* characteristics of Ni/GaAs-oxide/*n*-GaAs, Ni/GaAs-oxinitride/*n*-GaAs, etc, suggests that the deep levels are positively charged under the reverse bias condition, and then trap electrons when the bias approaches the flat-band voltage. Moreover, nitridation of the oxide film solves insufficient increase of high-frequency capacitance at a forward bias, which Passlack *et al.* theoretically derived as a sign of unpinning [14]. Frequency dependence of *C–V* curves of the Ni/GaAs-oxide/*n*-GaAs system, in a frequency range of 10 kHz $\sim$ 1 MHz, is small [12].

VII. Conclusion

We describe the fabrication and the characterization of GaAs MISFETs with nm-thin oxidized layers as the gate insulating layer. The oxidation was carried out by the UV and ozone process. The thickness of the oxidized layer was proportional to the square root of the oxidation time and was about 8 nm for 240 min oxidation time. From the *I–V* characteristics of the MIS diodes, the current suppression ratio of the MIS diode to the Schottky diode is 10^{-5} for 240 min oxidation time. The GaAs MISFETs with nm-thin oxidized layer formed by the UV and ozone process were fabricated. They could operate not only in the depletion mode but also in the accumulation mode up to 2 V and 3 V of the gate voltages for 3-nm-thick and 8-nm-thick oxidized layers, respectively, due to the current blocking effect of the oxidized layer. However, the I_D–V_D characteristics have hysteresis loop, and a large hysteresis was observed when the gate voltage is around the flat-band voltage. This result suggests the existence of interface states. The RF response of the GaAs MISFETs was measured, showing the current cutoff frequency of 6 GHz and the maximum oscillation frequency of 8 GHz with 1-μm-long gate length and 8-nm-thick oxidized layer. The quality improvement of the oxide layer is now being studied [12] and the results will be presented elsewhere along with some dielectric properties of the oxide layer.

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