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Description	

Characterization and Computation of Steiner Routing Based on Elmore's Delay Model

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SUMMARY As a remarkable development of VLSI technology, a gate switching delay is reduced and a signal delay of a net comes to have a considerable effect on the clock period. Therefore, it is required to minimize signal delays in digital VLSIs. There are a number of ways to evaluate a signal delay of a net, such as cost, radius, and Elmore's delay. Delays of those models can be computed in linear time. Elmore's delay model takes both capacitance and resistance into account and it is often regarded as a reasonable model. So, it is important to investigate the properties of this model. In this paper, we investigate the properties of the model and construct a heuristic algorithm based on these properties for computing a wiring of a net to minimize the interconnection delay. We show the effectiveness of our proposed algorithm by comparing ERT algorithm which is proposed in [2] for minimizing the maximum Elmore's delay of a sink. Our proposed algorithm decreases the average of the maximum Elmore's delay by 10–20% for ERT algorithm. We also compare our algorithm with an $\mathcal{O}(n^4)$ algorithm proposed in [15] and confirm the effectiveness of our algorithm though its time complexity is $\mathcal{O}(n^3)$.

key words: *Elmore's delay, Steiner tree, net, binary tree, Manhattan distance*

1. Introduction

For the design of high-performance VLSIs, minimizing interconnection delay becomes one of most significant issues since clock period is limited partly by interconnection delays of nets [2]. Interconnection delay can be approximately evaluated in linear time by computing cost (total wire length), radius (maximum wire length), or some objective function considering both capacitance and resistance.

The problem of minimizing cost is called Steiner minimal tree (SMT) problem. The problem is known to be NP-hard even if the host graph is restricted to being a grid [8]. This restricted version of the problem is called Steiner rectilinear minimal tree (SRMT) problem. Some papers, e.g., [9], [10], give theoretical analyses for the SMT problem. [10], [14] give linear time heuristic algorithms for SRMT and some other heuristics are also proposed in [12], [13], [16].

Since both capacitance and resistance have a sig-

nificant effect on the signal delay, some research studies have considered these parameters. The problem of minimizing both radius and cost is studied [1], [4], [17] and some tradeoffs between them are reported. [3] and [18] report on the SMT problem under the radius-preserved constraint or radius minimization problem under the cost constraint.

Elmore's delay model considers both wire capacitance and resistance [7]. Also, it is known that the delay for the model can be computed in linear time [19]. Some other research works also report on studies for Elmore's delay model [1], [2]. The problem of minimizing the Elmore's delay of a net is formulated as follows: The instance of the problem consists of

- sinks t located on (x_t, y_t) on a Manhattan plane together with its capacitance C_t ,
- a source s located on (x_s, y_s) on the plane together with the driver resistance R_d , and
- unit length capacitance c and unit length resistance r of a wire.

The solution of the problem is a rectilinear Steiner wiring S connecting the source and sinks, and its objective is to minimize the maximum Elmore's delay $t_{ED}(S)$ over all sinks.

In this paper, we investigate the problem of minimizing the maximum signal delay of wirings of a given net under Elmore's delay model. We give some properties on a Steiner vertex location, and show the relationships between these properties and the optimality of Elmore's delay theoretically. Then, we propose an $\mathcal{O}(n^3)$ heuristic algorithm for computing Steiner wirings of a given net N based on Elmore's delay model, where n is the number of sinks of N . We also compare our proposed algorithm with the ERT algorithm proposed in [2] which is also an $\mathcal{O}(n^3)$ heuristic algorithm for minimizing $t_{ED}(S)$. Our algorithm improves 10% of maximum Elmore's delay for the ERT algorithm in $0.5\ \mu\text{m}$ technology, and 16–20% in our estimated $0.1\ \mu\text{m}$ technologies. We also compared our proposed algorithm with an $\mathcal{O}(n^4)$ heuristic algorithm proposed in [15] and confirm the effectiveness of our algorithm.

2. Definition

A net N is the set of terminals $\{t_0, t_1, \dots, t_k\}$, where $t_0 = s$ is the *source* of N corresponding to the output of

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a gate and t_i 's ($i \geq 1$) are *sinks* corresponding to inputs of gates. Each terminal $t \in N$ allocated on a Manhattan plane has x - y coordinates (x_t, y_t) and $t \in N \setminus \{s\}$ has its capacitance C_t , where $x_t, y_t \in \mathbb{Z}$ or $x_t, y_t \in \mathbb{R}$. A Steiner wiring of N consists of some rectilinear wire segments on the plane which connect all terminals with the source. Our objective is to compute a wiring of N for minimizing interconnection delay under Elmore's delay model.

While, in a practical VLSI layout design, a number of modules and wires exist, and they become obstacles for a connection requirement of other nets, their appearances might depend deeply on the technology and design style. The major emphasis on this paper is on investigations of essential properties and the computation algorithm for Steiner routing based on Elmore's delay model without depending on specific technology or design style. Thus, we assume that two arbitrary points (x, y) and (x', y') on the plane can be connected by a wire segment with length $\text{MH}((x, y), (x', y')) \triangleq |x - x'| + |y - y'|$, the Manhattan distance between (x, y) and (x', y') .

In order to characterize a Steiner tree, we employ a binary tree representation (BTR) of a net N which helps us to represent the topology of a Steiner wiring of N . A BTR T of N is a (rooted) binary tree whose root is s and the outdegree of s is one, while all of the sinks $t \in N \setminus \{s\}$ appear as leaves. The indegree and outdegree of s are 0 and 1, each internal vertex 1 and 2, and each sink 1 and 0, respectively (see Fig. 1). Thus, the number of internal vertices is $|N| - 2$. Let $V(T)$ be the vertex set of T . For each vertex $v \in V(T) \setminus \{s\}$ of T except for the source, we denote the parent of v by $p(v)$. In Fig. 1, $v = p(w) = p(t_3)$, $w = p(t_1) = p(t_2)$, and $s = p(u)$.

We represent a Steiner wiring S of BTR T as a mapping ϕ^S (or simply denote by ϕ) of internal vertices of T to \mathbb{Z}^2 (or \mathbb{R}^2), where we assume $\phi(v) = (x_v, y_v)$ for $v \in V(T)$. We show an example of N , BTR T of N having internal vertices u and v , and Steiner wiring of T in Figs. 2(a), (b), and (c), respectively. In this Steiner wiring, v is located on the same point as t_3 by ϕ . When there are several possible ways to connect v and t_2 with minimum length rectilinear wiring, we represent such a wiring by a diagonal segment. For

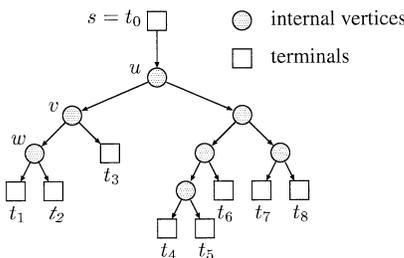


Fig. 1 BRT T of net N .

example, the segment connecting v and t_2 in Fig. 2(c) is represented as that in Fig. 2(d).

Let r and c be resistance and capacitance coefficients per unit length. For a vertex v except for s , let l_v be the length of the wire connecting v with its parent $p(v)$ in S . In Fig. 2(d), $l_{t_1} = 2$, $l_{t_2} = 3$, $l_{t_3} = 0$, $l_v = 2$, and $l_u = 1$. The capacitance C_v of v in a Steiner wiring S will be defined recursively as follows. If v is a sink, i.e., $v \in N \setminus \{s\}$, then C_v is given in the description of a problem instance. If v is an internal vertex, v has two children, say c_1 and c_2 . For such v , C_v is given as

$$C_v = C_{c_1} + C_{c_2} + c(l_{c_1} + l_{c_2}). \tag{1}$$

For the source s , it has exactly one child c_1 and $C_s = C_{c_1} + cl_{c_1}$. As a result, the capacitance of the source s is represented as

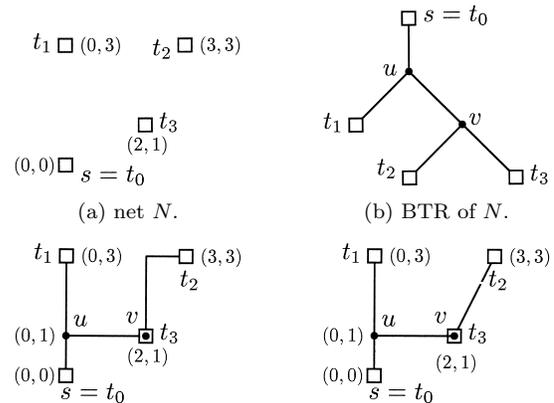
$$C_s = c \sum_{v \in V(T) \setminus \{s\}} l_v + \sum_{t \in N} C_t.$$

For example in Fig. 2(d), $C_v = c(l_{t_2} + l_{t_3}) + C_{t_2} + C_{t_3}$, $C_u = c(l_v + l_{t_1}) + C_v$, and $C_s = cl_u + C_u$. If we need to specify the Steiner wiring S explicitly, we denote l_v and C_v by l_v^S and C_v^S , respectively.

Using the driver resistance R_d , Elmore's delay at the source s is denoted by $\text{del}(s) = R_d C_s$. Elmore's delay $\text{del}(v)$ of a vertex $v \in V(T)$ of Steiner wiring S is denoted by

$$\text{del}(v) = R_d C_s + \sum_{u \in V(P_v) \setminus \{s\}} r l_u \left(\frac{cl_u}{2} + C_u \right), \tag{2}$$

where P_v is the path connecting s and v on T . If we need to specify S explicitly, we also denote it by $\text{del}^S(v)$. In this paper, we focus our attention on the maximum sink delay $\max_{v \in V(T)} \text{del}(v)$, and we denote it by $t_{\text{ED}}(S)$. A path P_v is called a *critical path* of S if $\text{del}(v) = t_{\text{ED}}(S)$. A Steiner wiring S of N is said to be *optimal* if its Elmore's delay is no greater than that of any other wiring for N .



(c) Steiner wiring S of N . (d) S with a diagonal segment.

Fig. 2 N and its Steiner wirings.

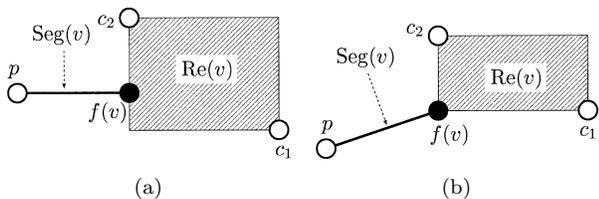


Fig. 3 Locations of v and its adjacent vertices.

For locations $(x_1, y_1), (x_2, y_2), \dots, (x_k, y_k)$, let

$$RC((x_1, y_1), (x_2, y_2), \dots, (x_k, y_k))$$

be the rectangle spanned by those locations, i.e., the rectangle area specified by

$$\left\{ (x, y) \mid \begin{array}{l} \min_{1 \leq i \leq k} x_i \leq x \leq \max_{1 \leq i \leq k} x_i, \\ \min_{1 \leq i \leq k} y_i \leq y \leq \max_{1 \leq i \leq k} y_i \end{array} \right\}.$$

Consider a vertex v , its children c_1 and c_2 and its parent p . Let $Re(v)$ be the rectangle area induced by c_1 and c_2 , i.e., $Re(v) = RC(\phi(c_1), \phi(c_2))$. Also, we let $f(v)$ be the position in $Re(v)$ nearest to p and let $Seg(v)$ be the line segment connecting $f(v)$ and the location of p (see Fig. 3). In particular, $f(v) = \phi(p)$ if $\phi(p) \in Re(v)$. Note that $Re(v)$, $f(v)$, and $Seg(v)$ are independent of the location of v . We sometimes denote them by $RC^S(\phi(c_1), \phi(c_2))$, $Re^S(v)$, $f^S(v)$, and $Seg^S(v)$, respectively, if we need to specify the Steiner wiring S explicitly.

3. Characterization of Elmore's Delay Model

In this section, we give some characterizations of Elmore's delay model, where we assume $\phi : V(T) \rightarrow \mathbb{R}^2$.

Lemma 1: For $v \in V(T)$ of BTR T , Elmore's delay $del(v)$ at v is monotonically increasing for the length of each wire l_w with $w \in V(T) \setminus \{s\}$.

Proof. Let v be a vertex of BTR T . Let us consider two Steiner wirings S and S' of T , where $l_v^S > l_v^{S'}$ and $l_u^S = l_u^{S'}$ for u with $u \neq v$ nor s . Then, $C_u^S \geq C_u^{S'}$ for all $u \in V(T)$ and $C_s^S > C_s^{S'}$. Thus, from (2), we have the lemma. \square

In the following, we assume that the length of a connection wire between u and v is given by the Manhattan distance between their locations. We now give some properties for a Steiner wiring.

Single vertex property (SVP): For a BTR T , $v \in V(T)$, and a wiring S of T , if location of v is in $Seg(v)$, v is said to satisfy Single vertex property.

Quasi-SVP (QSVP): For a BTR T , $v \in V(T)$, and a wiring S of T , if location of v is in $RC(\phi(p(v)), f(v))$, v is said to satisfy Quasi-single vertex property.

f-property for v: For $v \in N$, if $\phi^S(v) = f^S(v)$ then v is said to satisfy *f-property*.

f-property for S: S is said to satisfy *f-property* if all vertices $v \in V(T) \setminus N$ satisfy *f-property*.

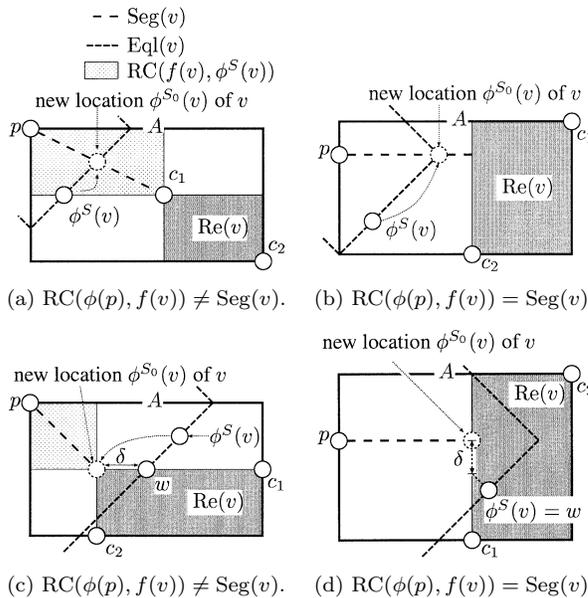


Fig. 4 Rectangles and the location of v .

3.1 Theorems with Respect to QSVP

The following lemma based on QSVP guarantees the existence of an optimal location of a vertex in $RC(\phi(p(v)), f(v))$:

Lemma 2: Let N be a net, T be its BTR, and S be an arbitrary Steiner wiring of T where at least one vertex $v \in V(T)$ does not satisfy SVP. Then, there exists a location $\varphi \in Seg(v)$ of v such that the wiring S_0 obtained from S by locating v on $\varphi = \phi^{S_0}(v)$ satisfies $del^{S_0}(u) \leq del^S(u)$ for all $u \in V(T)$. Also, if v does not satisfy QSVP in S , i.e., $\phi^S(v) \notin RC(\phi(p(v)), f(v))$, then $del^{S_0}(u) < del^S(u)$ for all $u \in V(T)$.

Proof. Let c_1 and c_2 be the children of v and p be the parent of v . Consider the rectangle area A induced by $\phi^S(c_1)$, $\phi^S(c_2)$, and $\phi^S(p)$, i.e., $A = RC(\phi^S(p), \phi^S(c_1), \phi^S(c_2))$. Then, there are two cases depending on whether the location of v is in A or not.

Case 1 $\phi^S(v) \in A$ (see Fig. 4).

Let $Eq(v)$ be the equi-distance line from p including v (broken line with narrow pitch in Fig. 4).

Case 1-1. $Eq(v)$ intersects with $Seg(v)$ (there are two cases that the area of $RC(\phi(p), f(v))$ is greater than 0 as shown in Fig. 4(a) and is 0, i.e., $RC(\phi(p), f(v)) = Seg(v)$ as shown in Fig. 4(b)).

If v satisfies QSVP in S , $l_u^{S_0} = l_u^S$ for all $u \in V(T) \setminus \{s\}$ (see Fig. 4(a)). Therefore, $del^{S_0}(u) = del^S(u)$. We now assume that v does not satisfy QSVP. We locate v at the intersection of $Seg(v)$ and $Eq(v)$, i.e., $\phi^{S_0}(v)$ as shown in Fig. 4(a) or (b)[†]. In this case, $l_{c_i}^{S_0} < l_{c_i}^S$ and

[†]If u has descendant v , $C_u^S > C_u^{S'}$. Otherwise, $C_u^S = C_u^{S'}$.

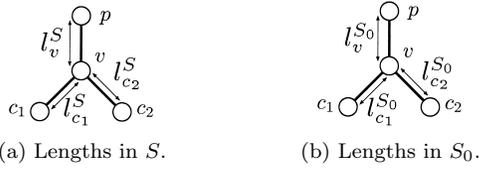


Fig. 5 Relation of lengths of $l_v, l_{c_1},$ and l_{c_2} .

$l_{c_j}^{S_0} = l_{c_j}^S$ for $i = 1$ and $j = 2$ or $i = 2$ and $j = 1$, where $i = 1$ and $j = 2$ in the figures. For other vertices $u \in V(T) \setminus \{v, c_1, c_2, s\}$, $l_u^{S_0} = l_u^S$. Thus, by Lemma 1, we have the lemma.

Case 1-2. $\text{Eq}(v)$ does not intersect with $\text{Seg}(v)$ (see Figs. 4(c) and (d)).

Let w be the location in $\text{Re}(v) \cap \text{Eq}(v)$ nearest to $\phi^S(v)$ (see Figs. 4(c) and (d)). (If $\phi^S(v) \in \text{Re}(v)$ then $w = \phi^S(v)$ as shown in Fig. 4(d)). For $i = 1, 2$,

$$\text{MH}(\phi(c_i), w) \leq \text{MH}(\phi(c_i), \phi^S(v)). \tag{3}$$

For every location $w' \in \text{Re}(v)$, $\text{MH}(\phi(c_1), w') + \text{MH}(\phi(c_2), w') = \text{MH}(\phi(c_1), \phi(c_2))$. Since $f(v), w \in \text{Re}(v)$, we have

$$\text{MH}(\phi(c_1), f(v)) = \text{MH}(\phi(c_1), w) + \delta \quad \text{and} \tag{4}$$

$$\text{MH}(\phi(c_2), f(v)) = \text{MH}(\phi(c_2), w) - \delta \tag{5}$$

for some δ with $|\delta| \leq \text{MH}(f(v), w)$. Without loss of generality, we can assume that $\delta > 0$. Let S_0 be the wiring obtained from S by locating v on $f(v)$. For S and S_0 , the length l_u with $u \in \{v, c_1, c_2\}$ is shown in Figs. 5(a) and (b), respectively. Since $\phi^{S_0}(v) = f(v)$, from (3), (4), and (5),

$$l_{c_1}^{S_0} \leq l_{c_1}^S + \delta, \tag{6}$$

$$l_{c_2}^{S_0} \leq l_{c_2}^S - \delta, \quad \text{and} \tag{7}$$

$$l_v^{S_0} \leq l_v^S - \delta. \tag{8}$$

From (6), (7), and (8), we have

$$l_{c_1}^{S_0} + l_v^{S_0} \leq l_{c_1}^S + l_v^S \quad \text{and} \tag{9}$$

$$l_v^{S_0} l_{c_2}^{S_0} \leq l_v^S l_{c_2}^S. \tag{10}$$

From (1) and $C_{c_i}^{S_0} = C_{c_i}^S$ for $i = 1, 2$,

$$C_v^{S_0} = C_{c_1}^S + C_{c_2}^S + c(l_{c_1}^{S_0} + l_{c_2}^{S_0}). \tag{11}$$

Then, from (9), $C_v^{S_0} \leq C_v^S$. Hence,

$$C_u^{S_0} \leq C_u^S \quad \forall u \in V(T). \tag{12}$$

From (6), (7), and (8) $C_s^{S_0} < C_s^S$ since $\delta > 0$ and $l_u^{S_0} = l_u^S$ for all $u \in V(T) \setminus \{s, v, c_1, c_2\}$. Therefore, we have

$$R_d C_s^{S_0} < R_d C_s^S. \tag{13}$$

We now consider Elmore's delay for each $u \in V(T)$. If path P_u does not include c_1 , for all $z \in V(P_u)$, $l_z^{S_0} \leq$

l_z^S . Thus, from (2), (12), and (13), $\text{del}^{S_0}(u) < \text{del}^S(u)$.

From (2), if we have $\text{del}^{S_0}(c_1) < \text{del}^S(c_1)$, we also have $\text{del}^{S_0}(u) < \text{del}^S(u)$ for all proper descendants u of c_1 since, for each proper descendant d of c_1 , $l_d^{S_0} = l_d^S$. The rest of the proof is to show $\text{del}^{S_0}(c_1) < \text{del}^S(c_1)$. Note that, for all $u \in V(P_{c_1}) \setminus \{v, c_1, s\} \subseteq V(T) \setminus \{v, c_1, c_2, s\}$, $l_u^{S_0} = l_u^S$. Therefore, from Lemma 1, (2), (12), and (13), we have

$$\begin{aligned} & (\text{del}^S(c_1) - \text{del}^{S_0}(c_1))/cr \\ & > \sum_{z \in \{v, c_1\}} \left(l_z^S \left(\frac{l_z^S}{2} + \frac{C_z^S}{c} \right) - l_z^{S_0} \left(\frac{l_z^{S_0}}{2} + \frac{C_z^{S_0}}{c} \right) \right) \\ & \geq \frac{(l_v^S)^2}{2} + l_v^S \left(\frac{C_{c_1}^S}{c} + \frac{C_{c_2}^S}{c} + l_{c_1}^S + l_{c_2}^S \right) \\ & \quad - \frac{(l_v^{S_0})^2}{2} - l_v^{S_0} \left(\frac{C_{c_1}^S}{c} + \frac{C_{c_2}^S}{c} + l_{c_1}^{S_0} + l_{c_2}^{S_0} \right) \\ & \quad + \frac{(l_{c_1}^S)^2}{2} + \frac{l_{c_1}^S C_{c_1}^S}{c} - \frac{(l_{c_1}^{S_0})^2}{2} - \frac{l_{c_1}^{S_0} C_{c_1}^S}{c} \end{aligned} \tag{14}$$

$$\begin{aligned} & = C_{c_1}^S ((l_v^S + l_{c_1}^S) - (l_v^{S_0} + l_{c_1}^{S_0}))/c \\ & \quad + ((l_v^S + l_{c_1}^S)^2 - (l_v^{S_0} + l_{c_1}^{S_0})^2)/2 \\ & \quad + C_{c_2}^S (l_v^S - l_v^{S_0})/c + (l_v^S l_{c_2}^S - l_v^{S_0} l_{c_2}^{S_0}) \\ & \geq 0. \end{aligned} \tag{15}$$

Inequality (14) follows from (11) and Inequality (15) follows from (8), (9), and (10). Thus, we have $\text{del}^{S_0}(c_1) < \text{del}^S(c_1)$.

Case 2 $\phi^S(v) \notin A$.

Let w be the location in A nearest to $\phi^S(v)$ and S'_0 be the Steiner wiring obtained from S_0 by changing the location of v to $w = \phi^{S'_0}(v)$. Then, $l_u^{S'_0} < l_u^S$ for $u \in \{v, c_1, c_2\}$ and $l_u^{S'_0} = l_u^S$ for $u \in V(T) \setminus \{s, v, c_1, c_2\}$. Hence, from Lemma 1, $\text{del}^{S'_0}(u) < \text{del}^S(u) \quad \forall u \in V(T)$. Since $\phi^{S'_0} \in A$, by similar arguments to Case 1, we have

$$\text{del}^{S_0}(u) \leq \text{del}^{S'_0}(u) \quad \forall u \in V(T).$$

Thus, we have $\text{del}^{S_0}(u) < \text{del}^S(u)$ for all $u \in V(T)$. \square
From Lemma 2, we have the following:

Theorem 1: Given a net N and its BTR T , there exists an optimal Steiner wiring S of T such that all internal vertices v satisfy QSVP. \square

Corollary 1: Given a net N , its BTR T , and a specified internal vertex $v \in V(T)$, there exists an optimal Steiner wiring S of T such that v satisfies SVP and all other internal vertices u satisfy QSVP.

Proof. Let S_0 be a minimum Elmore's delay wiring such that all internal vertices satisfy QSVP. From Theorem 1, such wiring S_0 exists. Let S be the new wiring obtained from S_0 by relocating v on the intersection of

[†]In the example of Fig. 4(a), v satisfies QSVP since $\phi^S(v) \in \text{RC}(\phi(p), f(v))$.

Seg(v) and Eq(v). Then, v comes to satisfy SVP in S . If all adjacent vertices to v satisfy QSVP, we have the corollary. If not, let $u \in \{p, c_1, c_2\}$ be the vertex which does not satisfy QSVP. In the new wiring S , for all vertices v , $l_v^S = l_v^{S_0}$. So, $t_{ED}(S) = t_{ED}(S_0)$, that is, S is also the minimum Elmore's delay wiring. However, this contradicts Lemma 2. \square

3.2 Steiner Wiring under f -Property

Intuitively, locating v on $f(v)$ makes Elmore's delay smaller. In fact, from Lemma 1, we have the following:

Theorem 2: \dagger If S is optimal and $v \in V(T)$ is not included in any critical path, then $\phi^S(v) = f^S(v)$, i.e., v satisfies f -property. \square

In this subsection, we consider Steiner wirings under f -property, i.e., Steiner wiring each of whose vertices satisfies f -property.

For $v \in V(T)$, we let p be the parent of v and let c_α and c_β be the children of v . Also, we let x_u and y_u be the x - and y -coordinates of vertex u , respectively, i.e., $\phi(u) = (x_u, y_u)$, for each $u = p, v, c_\alpha, c_\beta$. Then, for a Steiner wiring satisfying f -property,

$$x_v = \begin{cases} \min\{x_{c_\alpha}, x_{c_\beta}\} & \text{if } x_p \leq \min\{x_{c_\alpha}, x_{c_\beta}\} \\ \max\{x_{c_\alpha}, x_{c_\beta}\} & \text{if } x_p \geq \max\{x_{c_\alpha}, x_{c_\beta}\} \\ x_p & \text{if otherwise, and} \end{cases} \quad (16)$$

$$y_v = \begin{cases} \min\{y_{c_\alpha}, y_{c_\beta}\} & \text{if } y_p \leq \min\{y_{c_\alpha}, y_{c_\beta}\} \\ \max\{y_{c_\alpha}, y_{c_\beta}\} & \text{if } y_p \geq \max\{y_{c_\alpha}, y_{c_\beta}\} \\ y_p & \text{if otherwise.} \end{cases} \quad (17)$$

These equations imply that x_v is the middle value among x_p, x_{c_α} , and x_{c_β} and y_v is that among y_p, y_{c_α} , and y_{c_β} .

Two adjacent vertices property (TAVP): Consider BTR T of N , vertices v_1, v_2, p, c_1, c_2 , and $c_3 \in V(T)$ as shown in Fig. 6. The pair of vertices v_1 and v_2 is said to satisfy two adjacent vertices property if v_1 is located on the point in $RC(\phi(c_1), \phi(c_2), \phi(c_3))$ nearest to $\phi(p)$ and v_2 satisfies the f -property. (v_2 is located on the point in $RC(\phi(c_2), \phi(c_3))$ nearest to v_1 .)

Theorem 3: For a BTR T of N , consider two vertices v_1 and v_2 such that vertex v_1 has a parent p and children v_2 and c_1 , and vertex v_2 has children c_2 and c_3 (see Fig. 6). Let S^\dagger be an arbitrary Steiner wiring of T . Consider the set \mathbb{S} of Steiner wirings obtained

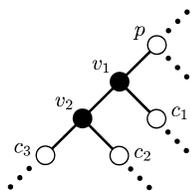


Fig. 6 v_i, p , and c_j in T .

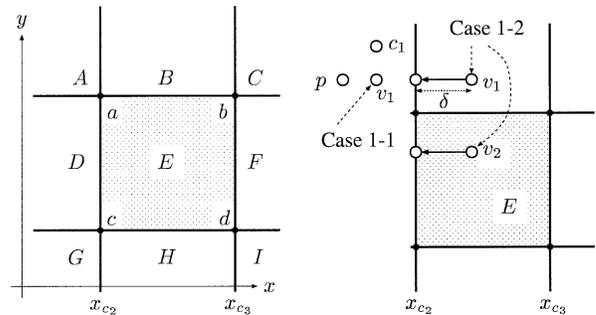
from S^\dagger by relocating only v_1 and v_2 such that both v_1 and v_2 satisfy f -property. Then, there exists a Steiner wiring $S \in \mathbb{S}$ in which the pair of v_1 and v_2 satisfies TAVP and, for each $S' \in \mathbb{S}$, $\text{del}^S(v) \leq \text{del}^{S'}(v)$ for all $v \in V(T)$.

Proof. As we can see in (16) and (17), x - and y -coordinates of v under f -property are independent of y - and x -coordinates of v , respectively. Hence, it is sufficient to show only one of x - or y -coordinates and we choose x -coordinates here. Without loss of generality, we can assume that $x_{c_2} \leq x_{c_3}$. Let S be the resultant wiring obtained from S^\dagger by changing only x -coordinates of v_1 and v_2 . We now divide the plane into nine regions from A to I separated by the bounding lines of $E = RC(\phi^{S^\dagger}(c_2), \phi^{S^\dagger}(c_3))$ (see Fig. 7(a)), where we assume that a vertex on a bounding line is included in both regions separated by the line and each intersection (a, b, c , and d in Fig. 7(a)) is included in four regions. We only consider two cases $x_p \leq x_{c_2}$ or $x_{c_2} \leq x_p \leq x_{c_3}$ since, for $x_p \geq x_{c_3}$, the similar arguments to $x_p \leq x_{c_2}$ hold.

Case 1 $x_p \leq x_{c_2}$, i.e., p is located in A, D , or G . Furthermore, we decompose the case into the following two sub-cases:

Case 1-1 $x_{c_1} \leq x_{c_2}$, i.e., c_1 is located in A, D , or G . We illustrate one example in the case of $y_{c_1} > y_p > \max\{y_{c_2}, y_{c_3}\}$ in Fig. 7(b). Since v_2 satisfies f -property, v_2 is located in $E = RC(\phi^{S^\dagger}(c_2), \phi^{S^\dagger}(c_3))$, i.e., $x_{v_2} \geq x_{c_2} \geq \max\{x_{c_1}, x_p\}$. So from (16), substituting $v = v_1$, x_{v_1} is the middle value among x_p, x_{c_1} , and x_{v_2} , and thus, $x_{v_1} = \max\{x_{c_1}, x_p\}$ and $x_{v_1} \leq x_{v_2}$. Therefore, again from (16) with $v = v_2$, $x_{v_2} = x_{c_2}$ since $x_{v_1} \leq x_{c_2} \leq x_{c_3}$. So, under f -property, x_{v_1} and x_{v_2} are determined uniquely.

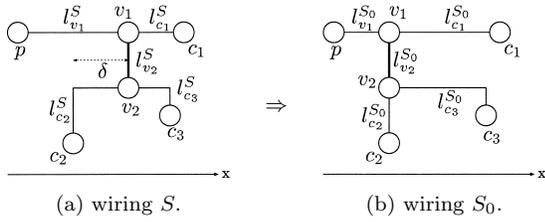
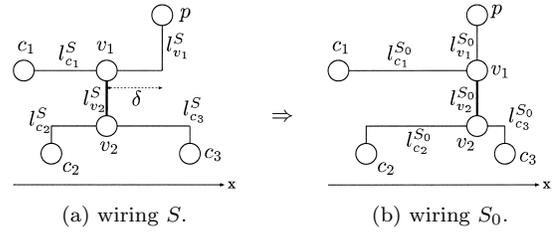
Case 1-2 $x_{c_1} \geq x_{c_2}$. Since $\phi(v_2) \in \text{Re}(v_2) = E$, $x_{v_2} \geq x_{c_2}$. Hence, $x_p \leq$



(a) Partition of the plane. (b) Vertex locations.

Fig. 7 Manhattan plane.

\dagger Theorem 2 does not refer to a vertex $v \in V(T)$ which is included in some critical path. In fact, we can construct a problem instance whose optimum Steiner wiring includes a vertex placed at a non-Hannan location, but on Seg(v) from Lemma 2. A similar remark is mentioned in [11].


Fig. 8 Wirings S_0 and S .

Fig. 9 Wirings S_0 and S in Case 2-1.

$\min\{x_{v_2}, x_{c_1}\}$. So, from (16) with $v = v_1$,

$$x_{v_1} = \min\{x_{v_2}, x_{c_1}\} \quad (18)$$

and then $x_{v_1} \geq x_{c_2}$. So, from (16) with $v = v_2$,

$$\begin{aligned} x_{v_2} &= \min\{x_{v_1}, x_{c_3}\} \\ &= \min\{x_{v_2}, x_{c_1}, x_{c_3}\}. \end{aligned}$$

This implies that $x_{v_2} \leq \min\{x_{c_1}, x_{c_2}\} \leq x_{c_1}$. Thus, from (18), $x_{v_1} = x_{v_2}$. As a result, we have

$$\max\{x_p, x_{c_2}\} \leq x_{v_1} = x_{v_2} \leq \min\{x_{c_1}, x_{c_3}\}. \quad (19)$$

Let $\delta = x_{v_1} - x_{c_2}$ (see Fig. 7(b)). We now show that, in this case, the resultant wiring S has minimum Elmore's delay for every vertex only if $\delta = 0$. Let S_0 be such a wiring with $\delta = 0$. (Note that v_1 and v_2 in S_0 satisfy TAVP for their x -coordinates.) From (19), for the wiring S ,

$$l_{v_1}^S = l_{v_1}^{S_0} + \delta, \quad (20)$$

$$l_{v_2}^S = l_{v_2}^{S_0}, \quad (21)$$

$$l_{c_1}^S = l_{c_1}^{S_0} - \delta, \quad (22)$$

$$l_{c_2}^S = l_{c_2}^{S_0} + \delta, \text{ and} \quad (23)$$

$$l_{c_3}^S = l_{c_3}^{S_0} - \delta \quad (24)$$

(see Fig. 8). Then, $C_{v_1}^S = C_{v_1}^{S_0} - c\delta$, and $C_u^S = C_u^{S_0}$ for all other vertices u . For a vertex v and its parent p_v , we let $\text{ED}^{S^*}(v) = \text{del}^{S^*}(v) - \text{del}^{S^*}(p_v)$, i.e., $\text{ED}^{S^*}(v) = rl_v^{S^*}(\frac{cl_p^{S^*}}{2} + C_v^{S^*})$, where $S^* \in \{S, S_0\}$. Also, we let $\text{Diff}(v) = \text{del}^S(v) - \text{del}^{S_0}(v)$. Then, from (20) and $C_{v_1}^S = C_{v_1}^{S_0} - c\delta$, we have

$$\text{Diff}(v_1) = r\delta C_{v_1}^{S_0} - \frac{rc\delta^2}{2}. \quad (25)$$

Similarly, noting $C_u^S = C_u^{S_0}$ for $u \neq v_1$ and (21) to (24), we have

$$\text{Diff}(v_2) \geq 0, \quad (26)$$

$$\text{Diff}(c_1) \geq -r\delta(C_{c_1}^{S_0} + cl_{c_1}^{S_0}) + \frac{rc\delta^2}{2}, \quad (27)$$

$$\text{Diff}(c_2) \geq r\delta(C_{c_2}^{S_0} + cl_{c_2}^{S_0}) + \frac{rc\delta^2}{2}, \text{ and} \quad (28)$$

$$\text{Diff}(c_3) \geq -r\delta(C_{c_3}^{S_0} + cl_{c_3}^{S_0}) + \frac{rc\delta^2}{2}. \quad (29)$$

In addition,

$$C_{v_1}^{S_0} = C_{c_1}^{S_0} + C_{v_2}^{S_0} + c(l_{c_1}^{S_0} + l_{v_2}^{S_0}) \quad (30)$$

$$> C_{c_2}^{S_0} + C_{c_3}^{S_0} + c(l_{c_2}^{S_0} + l_{c_3}^{S_0}). \quad (31)$$

From (25), (27), and (30),

$$\begin{aligned} \text{del}^S(c_1) - \text{del}^{S_0}(c_1) &= \text{Diff}(v_1) + \text{Diff}(c_1) \\ &\geq r\delta(C_{v_2} + cl_{v_2}) \\ &> 0. \end{aligned}$$

Similarly, from (25), (26), (28), and (31), we have $\text{del}^{S_0}(c_2) < \text{del}^S(c_2)$ and, from (25), (26), (29), and (31), we have $\text{del}^{S_0}(c_3) < \text{del}^S(c_3)$. For other vertices v , clearly, $\text{del}^{S_0}(v) \leq \text{del}^S(v)$. Thus, the x -coordinates of v_1 and v_2 of S are determined uniquely.

Case 2 $x_{c_2} \leq x_p \leq x_{c_3}$.

We only need to consider the following two cases since, if $x_{c_1} \geq x_{c_3}$, similar arguments to Case 2-1 ($x_{c_1} \leq x_{c_2}$) hold:

Case 2-1 $x_{c_1} \leq x_{c_2}$.

From (16) with $v = v_2$, $x_{v_2} \geq x_{c_2}$ and then $x_{c_1} \leq x_{v_2}$. If $x_{v_2} > x_p$ then from (16) with $v = v_1$, $x_{v_1} = x_p$. However, from (16) with $v = v_2$, $x_{v_1} = x_{v_2}$ and this contradicts $x_{v_1} = x_p < x_{v_2}$. Therefore, $x_{v_2} \leq x_p$.

From (16) with $v = v_1$, $x_{v_1} = x_{v_2}$ since $x_{c_1} \leq x_{v_2} \leq x_p$. Thus, $x_{c_1} \leq x_{c_2} \leq x_{v_1} = x_{v_2} \leq x_p \leq x_{c_3}$ (cf., (19) and see Fig. 9). Put $\delta = x_p - x_{v_1}$. Then, changing the situations of c_2 and c_3 , we have the same equations from (20) to (24). Thus, by similar arguments to Case 1-2, we have the theorem for x -coordinates.

Case 2-2 $x_{c_2} \leq x_{c_1} \leq x_{c_3}$.

Without loss of generality we can assume that $x_{c_1} \leq x_p$. By similar arguments to Case 1-2, $x_{c_2} \leq x_{c_1} \leq x_{v_1} = x_{v_2} \leq x_p \leq x_{c_3}$ (cf., (19)) and thus we have the theorem for x -coordinates. As mentioned above, the same arguments hold for y -coordinates. Thus, we have the theorem. \square

4. Proposed Algorithm

In this section, we describe our proposed algorithm which consists of two parts: the first one (Init-algorithm) computes an initial Steiner wiring of a given net and constructs corresponding initial BTR, the second one (RC-algorithm) reconfigures the BTR and

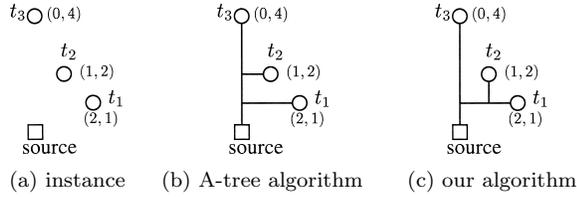


Fig. 10 Disadvantage of A-tree algorithm.

Steiner wiring. The time complexity of our proposed algorithm is $\mathcal{O}(|N|^3)$. The Init-algorithm is quite similar to the A-tree algorithm proposed in [5] (and [6]), where Init-algorithm combines the nearest subtrees first but A-tree algorithm combines the subtree farthest from the source first. Since the farther sinks from the source tend to become a critical sink in A-tree algorithm, *under Elmore's delay model*, it has the following disadvantage for a three-sink net as shown in Fig. 10. For the instance in Fig. 10(a), A-tree algorithm outputs the wiring shown in Fig. 10(b) and our algorithm outputs that in Fig. 10(c). If each sink has the same capacitance, Fig. 10(c) has a smaller delay than does (b). Init-algorithm also has a similar objective to the algorithm proposed in [18], while the algorithm in [18] considers the problem for only one-quadrant sinks.

4.1 Initial Steiner Wiring

In this subsection, we give an algorithm, called Init-algorithm, for computing BTR T from a given net N and a Steiner wiring S of T (that is, ϕ of S). Init-algorithm generates a wiring satisfying the following two conditions:

- each internal vertex satisfies SVP, f -property, and TAVP, and
- each terminal t is connected along one of the shortest routings connecting the source and t .

The first condition (a) is based on Theorem 3 and the second (b) is based on radius-preserved wiring, one of the traditional well-known objectives.

We assume that the root s of T (the source of N) is located on $(0,0)$. We construct the initial wiring by combining two subtrees recursively. Leaves of each subtree are sinks. Initially, each subtree is trivial, i.e., consisting of a sink in $N \setminus \{s\}$.

The body of Init-algorithm is as follows: We choose the pair of subtrees having minimum distance and then combine them. While the number of subtrees is not one, repeat this operation. After combining all subtrees, we then add the source s to the resultant tree T' with root s' and add an arc (s, s') .

The distance and "combining operation" are defined as follows, where we consider two *sub-wirings* whose BTRs are T_1 and T_2 , and let s_i be the root of T_i for $i = 1, 2$:

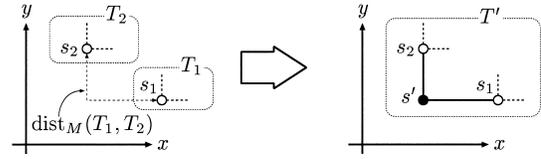


Fig. 11 Combining subtrees in the same quadrant.

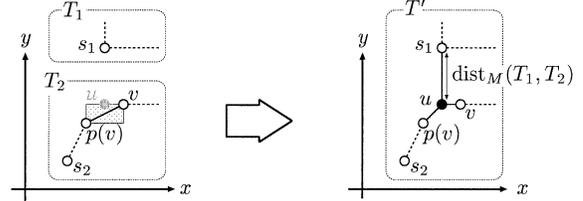


Fig. 12 Combining subtrees in the same quadrant.

Case 1 s_1 and s_2 are located in the same quadrant, i.e., $x_{s_1}x_{s_2} \geq 0$ and $y_{s_1}y_{s_2} \geq 0$.

As an example, we consider the case that $x_{s_1}, x_{s_2}, y_{s_1}, y_{s_2} \geq 0$. Without loss of generality, we can assume that $|x_{s_1}| \geq |x_{s_2}|$.

If $|y_{s_1}| \leq |y_{s_2}|$, $\text{dist}_M(T_1, T_2) = |x_{s_2} - x_{s_1}| + |y_{s_1} - y_{s_2}|$. If we combine T_1 and T_2 in this situation, the new subtree T' is constructed as follows: add a new vertex s' and two arcs (s', s_1) and (s', s_2) to $T_1 \cup T_2$ (see Fig. 11), and then locate s' on (x_{s_2}, y_{s_1}) , i.e., s' is located on the point in $\text{RC}(\phi(s_1), \phi(s_2))$ nearest to $(0,0)$. s' is the root of the new subtree.

If $|y_{s_1}| > |y_{s_2}|$, we choose a vertex $v \in V(T_2)$ which minimizes $\min_{\varphi \in \text{RC}(\phi(v), \phi(p(v)))} \text{MH}(\varphi, \phi(s_1))$ (see Fig. 12). Note that if T_2 consists of one vertex v then $\varphi = \phi(v)$. Using such v , the distance between T_1 and T_2 is defined as

$$\text{dist}_M(T_1, T_2) = \min_{\substack{\varphi \in \text{RC}(\phi(v), \phi(p(v))) \\ v \in V(T_2)}} \text{MH}(\varphi, \phi(s_1)).$$

We construct a new subtree T' from T_1 and T_2 in this situation as follows: delete an arc $(p(v), v)$ and add a new vertex u and three arcs $(p(v), u)$, (u, v) , and (u, s_1) , where u is located on φ (see Fig. 12). s_2 is the root of the resultant subtree T' .

Case 2 s_1 and s_2 are located in the adjacent quadrants, i.e., $x_{s_1}x_{s_2} < 0$ and $y_{s_1}y_{s_2} \geq 0$ or $y_{s_1}y_{s_2} < 0$ and $x_{s_1}x_{s_2} \geq 0$.

The distance is defined as

$$\begin{aligned} \text{dist}_M(T_1, T_2) &= \text{MH}(\phi(s_1), \phi(s_2)) \\ &= |x_{s_1} - x_{s_2}| + |y_{s_1} - y_{s_2}|. \end{aligned}$$

We can assume without loss of generality that $x_{s_1} > 0$, $x_{s_2} < 0$, and $|y_{s_1}| \geq |y_{s_2}|$ (see Fig. 13, where we assume $y_{s_1}, y_{s_2} \geq 0$ in this figure). We construct T' from T_1 and T_2 in this situation by adding a new vertex s' located on $(0, \min\{y_{s_1}, y_{s_2}\})$ and two arcs (s', s_1) and (s', s_2) . s' is the root of the resultant subtree T' .

Case 3 Otherwise, i.e., $x_{s_1}x_{s_2} < 0$ and $y_{s_1}y_{s_2} < 0$.
The distance is defined as

$$\text{dist}_M(T_1, T_2) = \text{MH}(\phi(s_1), \phi(s_2)).$$

We construct T' from T_1 and T_2 in this situation by adding a new vertex s' located on $(0, 0)$ and arcs (s', s_1) and (s', s_2) . s' is the root of the resultant subtree T' .

4.2 Reconstruction of the BTR

We now describe an algorithm for reconfiguring BTR T , say RC-algorithm. The algorithm is applied to T obtained by Init-algorithm. In this algorithm, each vertex is located to satisfy f -property.

Single reconfiguring operation for a vertex A vertex $v \in V(T)$, except the root and its child, is given as the input. Let p_v and w be the parent and brother of v , respectively.

- Remove the subtree rooted at v together with p_v from the tree T (see Fig. 14(a)).
- Find the vertex u and its parent q with $\phi(q) \in \text{RC}(\phi(v), \phi(s))^\dagger$ such that the shortest connection with v can be accomplished, i.e., the distance between the location of v and the nearest location to v in the rectilinear area spanned by u and q .
- If such u exists, insert p_v into the arc (q, u) (see Fig. 14(b)) and locate p_v to satisfy f -property.

If the maximum Elmore's delay of the resultant Steiner wiring T' becomes smaller, we update the Steiner tree T to T' . If otherwise, we reject T' and restore T .

Reconfiguring algorithm (RC-algorithm) We apply the Single reconfiguring operation to the vertices v whose Manhattan distance $\text{MH}(\phi(v), (0, 0))$ from $\phi(s)$ is greater than 0 such that the vertex having the smallest Manhattan distance from s is first.

Since the new location of p_v in Single reconfiguring algorithm operation for v has no greater Manhattan

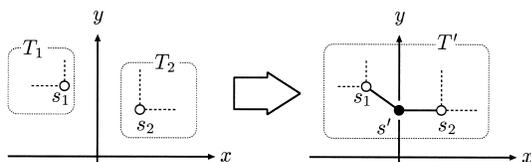


Fig. 13 Combining subtrees in adjacent quadrants.

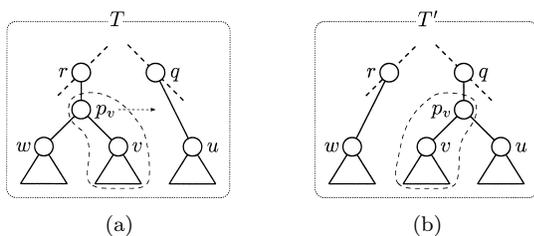


Fig. 14 Reconfiguration of binary tree.

distance than that of v (and other vertex locations are not changed), all Steiner points and terminals are subjected to this operation at most once. As a result, each p_v is located on the point satisfying the f -property. The resultant wiring satisfies SVP and TAVP.

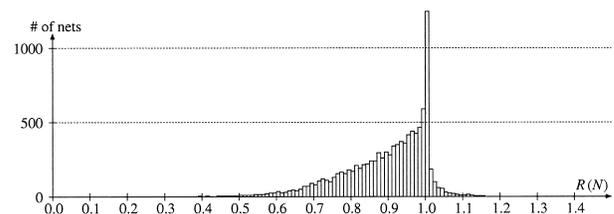
5. Experimental Result

We compare our proposed algorithm with the ERT algorithm described in [2] by comparing the Elmore's delay for randomly generated nets. The time complexity of both algorithms is $\mathcal{O}(|N|^3)$.

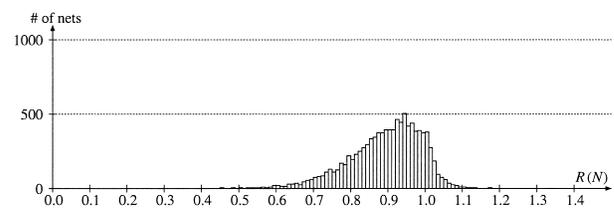
5.1 0.5 μm Technology

We apply our algorithm and the ERT algorithm to 10-, 20-, and 30-sink nets under the following technology: $\lambda = 0.5 \mu\text{m}$ (the unit length of x - y coordinate is $2\lambda = 1.0 \mu\text{m}$), $R_d = 270.0 \Omega$, $r = 0.112 \Omega/\mu\text{m}$, $c = 0.039 \text{fF}/\mu\text{m}$, $C_t = 1.0 \text{fF}$ (identical sink load capacitance), and the chip size is $10 \text{mm} \times 10 \text{mm}$. (We refer to the parameters in [1].)

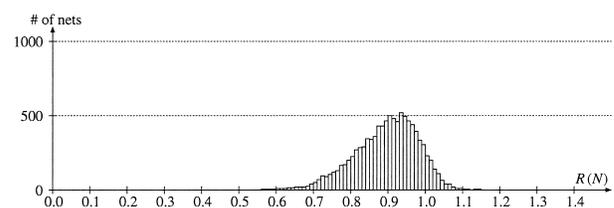
For each number of sinks, we randomly generate 10^4 nets N . We will compare ERT and our proposed algorithms by computing $R(N) = t_{\text{ED}}(T_o^N)/t_{\text{ED}}(T_{\text{ERT}}^N)$, where T_o^N is the Steiner wiring obtained by our algorithm and T_{ERT}^N is obtained by the ERT algorithm. Figures 15 (a), (b), and (c) show the distributions of the



(a) for 10-sink nets.



(b) for 20-sink nets.



(c) for 30-sink nets.

Fig. 15 Distributions of $R(N)$.

[†]This condition guarantees the radius-preserved wiring.

Table 1 Experimental results for 10- and 20-sink nets.

# of sinks	$R(N)$		
	best	avg	worst
10	0.3947	0.8968	1.1594
20	0.4560	0.8952	1.1702
30	0.5643	0.8955	1.1482

number of wires with respect to $R(N)$ for 10-, 20-, and 30-sink nets respectively. Each column shows the number of nets N satisfying $0.01i \leq R(N) < 0.01(i+1)$ for each integer i . Table 1 gives the maximum, average, and minimum ratios $R(N)$ over 10^4 nets. Based on the average ratios, our algorithm yields a 10% improvement over the ERT algorithm under the Elmore's delay model. Thus, we can conclude that our proposed algorithm is much better than the ERT algorithm in the case of $0.5 \mu\text{m}$ technology. The average runtimes of our proposed algorithm (measured by averaging runtimes of 10^5 runs) for $|N| - 1 = 10, 20,$ and 30 are 22×10^{-5} sec, 113×10^{-5} sec, and 307×10^{-5} sec, respectively, when the algorithm is implemented on a Pentium-II 266 processor with 128 MB RAM using C-language on the Linux OS.

5.2 Our Estimated $0.1 \mu\text{m}$ Technologies

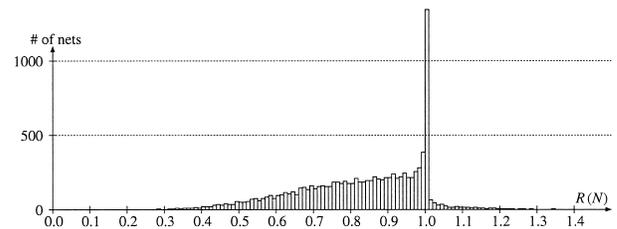
We also compare those algorithms under the our estimated $0.1 \mu\text{m}$ technologies. It should be noted that those parameters may be different from the practical ones. Since we evaluate the Elmore delay for randomly generated nets, only the ratios between $R_d/r : C_t/c : W$ (and λ) are important, where W is the length of the chip boundary.

We estimate the parameters of $1/5$ scaled technology as follows: $R'_d = \alpha R_d/5$, $C'_t = C_t/5$, $r' = 25r$, $c' = \beta c$, and $\lambda' = 0.2\lambda$, where we set $2 \leq \alpha \leq 4$ and $1 \leq \beta \leq 2$. The width and height of the chip are also set to $1/5$ times. We apply both algorithms with some α 's and β 's to 10^4 randomly generated nets. We summarize the result in Table 2. As examples, we show the distributions of the case that $\alpha = 3$ and $\beta = 1.5$ for 10-, 20-, and 30-sink nets in Figs. 16(a), (b), and (c), respectively. In this technology, our algorithm improves the average Elmore's delay by 16.5–20%. From the viewpoint of the average ratios, our proposed algorithm is also much better than the ERT algorithm. From the viewpoint of the distribution of $R(N)$ in Fig. 16, $R(N)$ is greater than 1 for only a few nets N though there exists a 30-sink net N whose ratio $R(N)$ is more than 139% in the estimated $0.1 \mu\text{m}$ technologies. Therefore, we can conclude that our proposed algorithm is much better than the ERT algorithm in the estimated $0.1 \mu\text{m}$ technologies.

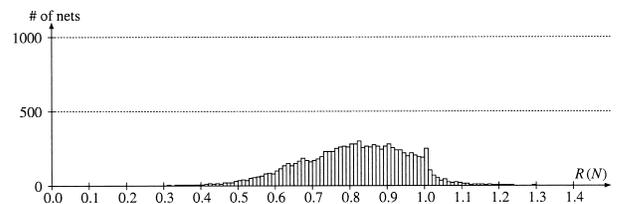
One of the disadvantages of our algorithm is that our algorithm outputs only radius-preserved wirings and does not always minimize the total wire length. Therefore, our algorithm outputs worse solutions than

Table 2 $R(N)$ for estimated $0.1 \mu\text{m}$ technologies.

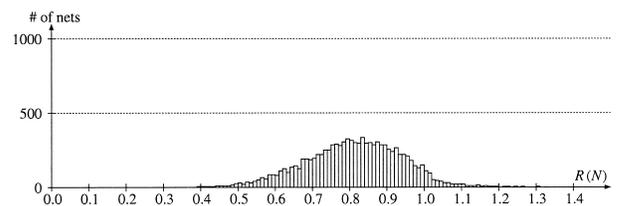
# of sinks	0.1 μm		$R(N)$		
	α	β	best	avg	worst
10	2	1.0	0.2611	0.8210	1.3345
		1.5	0.1946	0.8230	1.3058
		2.0	0.2777	0.8216	1.2686
	3	1.0	0.2670	0.8315	1.2982
		1.5	0.2872	0.8296	1.3473
		2.0	0.2928	0.8294	1.2880
	4	1.0	0.2869	0.8341	1.3561
		1.5	0.2995	0.8343	1.3214
		2.0	0.2790	0.8339	1.2618
20	2	1.0	0.3098	0.8018	1.3591
		1.5	0.3257	0.8055	1.3466
		2.0	0.3616	0.8014	1.3067
	3	1.0	0.3203	0.8108	1.2621
		1.5	0.3132	0.8123	1.2999
		2.0	0.2736	0.8145	1.2537
	4	1.0	0.3441	0.8221	1.2639
		1.5	0.3261	0.8207	1.2779
		2.0	0.3409	0.8226	1.2744
30	2	1.0	0.3284	0.8044	1.2682
		1.5	0.3386	0.7995	1.3920
		2.0	0.3506	0.8286	1.3203
	3	1.0	0.3813	0.8122	1.2507
		1.5	0.3997	0.8110	1.3009
		2.0	0.3755	0.8114	1.2847
	4	1.0	0.4173	0.8221	1.2086
		1.5	0.3829	0.8199	1.2523
		2.0	0.3213	0.8206	1.3303



(a) For 10-sink nets.



(b) For 20-sink nets.



(c) For 30-sink nets.

Fig. 16 Distributions of $R(N)$.

Table 3 $R(N)$ of 20-sink nets for the algorithm proposed in [15].

Tech.	α	β	best	avg	worst
0.5 μm	—	—	0.9010	0.9842	1.0310
0.1 μm	2	1.0	0.7877	1.0055	1.2014
		1.5	0.7534	0.9955	1.1670
		2.0	0.7136	0.9868	1.1514
	3	1.0	0.8246	0.9957	1.1339
		1.5	0.7982	0.9869	1.1014
		2.0	0.7764	0.9775	1.0897
	4	1.0	0.8526	0.9907	1.0766
		1.5	0.8043	0.9828	1.0921
		2.0	0.8083	0.9767	1.0717

the ERT algorithm for some nets as seen in Tables 1 and 2.

5.3 Comparison with an $\mathcal{O}(n^4)$ Algorithm

We also compare our proposed algorithm with the algorithm proposed in [15], which we call TBT, for 10^5 20-sink nets in 0.5 μm technology and our estimated 0.1 μm technologies. TBT uses an algorithm for finding an SRMT as a subprocedure and the time complexity of TBT is $\mathcal{O}(n^4 + n\tau(n))$, where $\tau(n)$ is the time complexity of a subprocedure algorithm for finding an SRMT. Hence, we use an $\mathcal{O}(n^3)$ algorithm for finding an SRMT, and construct a TBT with its time complexity $\mathcal{O}(n^4)$. An advantage of our algorithm over TBT may be that, subtrees are moved in our algorithm though only one sink is moved in TBT. The results are shown in Table 3. As evident from Table 3, if α and β become larger (resp. smaller), the results of our algorithm become better (resp. worse) than those of TBT. The detailed analysis of the results is left for future work.

6. Conclusion

In this paper, we investigate the maximum delays of wirings of a net under the Elmore's delay model. We propose two main characterizations of the model; QSVP and f -property. As a theoretical result, we show the relationship between QSVP and optimal wirings, that is, there exists an optimal wiring satisfying QSVP. We also propose an algorithm based on our theoretical results, and the experimental result reveals that the algorithm displays better performance than the $\mathcal{O}(n^3)$ ERT algorithm and almost the same performance as the $\mathcal{O}(n^4)$ TBT algorithm in the cases of 0.5 μm technology and our estimated 0.1 μm technologies under the Elmore's delay model.

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