N-channel field effect transistors with fullerene thin films and their application to a logic gate circuit

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Abstract

N-channel field effect transistors (FETs) were fabricated with thin films of C_{60} and Dy@C_{82}. A typical enhancement-type FET property was observed in C_{60} FET above 220 K. The mobility of C_{60} FET increased with increasing temperature. This fact suggests hopping transport as the conduction mechanism, with the activation energy of 0.29 eV. The Dy@C_{82} FET was found to be a normally-on type FET, which has a property different from that for C_{60} and C_{70} FETs. A complementary metal oxide semiconductor (CMOS) logic gate circuit was first fabricated with C_{60} and pentacene thin-film FETs.

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1. Introduction

Field effect transistors (FETs) with thin films of organic molecules have been studied by many groups [1,2]. The advantages of the FETs with organic molecules (organic FETs) over those with conventional inorganic materials are structural flexibility, low-temperature processing, large-area coverage and low cost. Potential applications of organic FETs to low-end data storage [1,2], switching devices for active displays [1-4], and especially to logic circuits [5-7], have been discussed in the recent literature. The current effort is devoted to increment of the mobilities, μ, of organic FETs for use in devices requiring high switching speed. At this moment the μ value as high as 1.5 cm^2 V^{-1} s^{-1} for p-channel pentacene FET has been achieved [8]. The temperature dependence of μ in the pentacene FET indicated hopping transport when the μ at room temperature was 0.3 cm^2 V^{-1} s^{-1}; the activation energy, E_a, was 3.8 x 10^{-2} eV [9].

An n-channel FET with a thin film of C_{60} was first fabricated in 1995 [10]; it had μ and threshold voltage, V_T, estimated to be 8 x 10^{-2} cm^2 V^{-1} s^{-1} and 15 V, respectively. The μ value of the C_{60} FET has recently been improved to 0.56 cm^2 V^{-1} s^{-1} by achieving the device fabrication and the FET-characteristics measurement under 10^{-10} Torr without exposure to air [11]. This result indicates that fullerene thin-film FETs can play an important role in science and technology of organic FETs.

The electronic properties of metallofullerenes have also been studied by spectroscopic and transport measurements by provision of suitable solid samples [12-15]. Small gap energies, E_g of 0.4 and 0.2 eV for Ce@C_{82} and Dy@C_{82}, respectively, estimated by resistivity measurements, have shown that they are semiconductor-like materials [14,15]. Furthermore, the valences of Dy and Ce atoms are determined to be both +3 from the XANES spectra [12,15]. However, no FETs with metallofullerenes have yet been studied. The present letter reports on the fabrication of a FET with a Dy@C_{82} thin-film, the transport properties of the C_{60} FET, and CMOS NOT logic circuits fabricated with C_{60} and pentacene thin-film FETs.

2. Experimental

A schematic structure of fullerene and pentacene FETs is shown in Fig. 1(a); the bottom-contact device is adopted. Commercially available C_{60} (99.98%) and pentacene (99.9 %) were used for fabrication of thin films. The sample of Dy@C_{82} (99.5 %) was obtained according to the method described elsewhere [12]. The SiO_2/Si substrate was washed with acetone by ultrasonic irradiation prior to fabrication of a device. Gold electrodes, fullerenes, and pentacene were formed on the SiO_2/Si substrate by thermal deposition at 10^{-6} – 10^{-7} Torr; the SiO_2/Si substrate was not heated during thermal deposition. The FET devices were exposed to air for $\approx$1 h when they were moved from the vacuum chamber for thermal deposition to the vacuum cell for measurements of FET-characteristics. The characteristics of the FET devices and the logic circuit were measured at 10^{-6} Torr after annealing of the FET devices at 120 ℃ and 10^{-6} Torr for 12 h.

3. Results and discussion

3.1. Normally-off FET with C_{60} thin film

The plots of I_D-V_{DS} for FETs with 200 and 10 nm C_{60} films, fabricated under the same conditions, are shown in Figs. 2(a) and (b). The μ values for the C_{60} FET with 200 and 10 nm films were estimated from the I_D-V_G plot at V_{DS} = 5 V (linear region) and from the $I_D^{1/2}$-V_G plot at 70 V (saturation region). The I_D -V_G plot at V_{DS} = 5 V for the C_{60} FET with 10 nm film is shown in Fig. 2(c) as an example. These values were estimated by the formula adopted for the MOSFET [16]. The μ and V_T values for these C_{60} FETs are listed in Table 1. The μ values are found to increase drastically with decreasing thickness to 10 nm. The μ values for the C_{60} FET in the 10 nm film, 1.0 x 10^{-1} cm^2 V^{-1} s^{-1} from the linear region and 1.4 x 10^{-1} cm^2 V^{-1} s^{-1} from the saturation region, are the highest in the present observations; they are comparable to that reported by Haddon et al. [10]. The V_T values, estimated to be 11 V from the linear region (V_{DS} = 5 V) and 10 V from the saturation region (V_{DS} = 70 V), are very low. This result implies that this FET is a device with high performance.

The carrier density, N, was estimated to be 3.7 x 10^{12} cm^{-2} at V_G = 70 V from CV_G / e for

the 10 nm film, while the N value was estimated to be 5.0 x 10^{12} cm^{-2} at V_G = 70 V for the 200 nm film. Here C (= ε_{0x}/d) and e denote capacitance per unit area of the SiO_2 layer and elementary charge, respectively, and ε_{0x} and d denote gate dielectric constant and thickness of SiO_2, respectively. Furthermore, the N was estimated to be 3.2 x 10^{12} cm^{-2} from σ /μe for the 10 nm film, being consistent with that estimated from CV_G / e. The channel conductivity, σ, was estimated to be 5.1 x 10^{-2} S cm^{-1} at V_G = 70 V and V_{DS} = 10 V (linear region). The σ observed at V_G = 70 V corresponds to conductivity of the channel region electron-induced from the gate dielectrics. The thickness of the channel region is known to be 4 – 40 nm for the MOSFET [17]. Here we present a model that impurities such as O_2 and H_2O can be effectively removed from the channel region by annealing of the 10 nm FET at 120 ℃ under ≈10^{-6} Torr, because the film thickness is nearly equal to that of the channel region. Such a removal of impurity should lead to a decrease in the trapping sites of the channel region and an increase in the μ value. In the present study, no FET characteristics were observed in the C_{60} FET without annealing of the device under vacuum once the device was exposed to air. Consequently, we note that the effective removal of impurity gases is essential to realize a proper performance of the FET device.

On the other hand, a further decrease in the thickness showed a drastic decrease in μ from 1.0 x 10^{-1} cm^2 V^{-1} s^{-1} for 10 nm to 5.5 x 10^{-3} cm^2 V^{-1} s^{-1} for 5 nm. No C_{60} granules were clearly observed in the AFM image for the 5 nm film. This fact suggests breaking of the channel through C_{60} granules. This breaking should cause a significant decrease in μ, being consistent with the observations reported above.

3.2. Normally-on FET with Dy@C_{82} thin film

In the I_D-V_{DS} plots in the Dy@C_{82} thin-film FET at 295 K, shown in Fig. 3(a), the I_D is 760 nA at V_{DS} = 110 V and V_G = 0 V. Thus high enough I_D is obtained even when no carrier is induced into the Dy@C_{82} interface from the dielectric gate. This I_D originates from the intrinsic bulk current of Dy@C_{82}, being different from the case for the C_{60} and C_{70} FETs. The

I_D increases linearly with increasing V_{DS} as well as V_G. These results imply that the Dy@C_{82} FET is an n-channel normally-on type FET, in contrast to the C_{60} FET, which is an n-channel enhancement and a normally-off type FET. In Dy@C_{82} three-electron transfer occurs from the Dy atom to the C_{82} cage as in $Dy^{3+}@C_{82}^{3-}$. Therefore, the carriers in the Dy@C_{82} FET at V_G = 0 V can be ascribed to the electrons on the C_{82} cage transferred from Dy. The absence of saturation in the I_D-V_{DS} plots for the Dy@C_{82} thin-film FET can be ascribed to the high carrier concentration due to the electrons induced by the gate voltage and those contributing to the intrinsic bulk current. The N value induced from the dielectric gate is estimated to be 5.3 x 10^{12} cm^{-2} at V_G = 140 V from CV_G /e. This value solely reflects the electron density induced from the gate dielectrics. The actual carrier concentration should be higher because of the contribution of the electrons associated with the bulk current.

The I_D-V_G plot at V_{DS} = 40 V (linear region) is shown in Fig. 3(b). The μ value is estimated to be 8.9 x 10^{-5} cm^2 V^{-1} s^{-1} from the I_D-V_G plot. The normally-on property is directly associated with the existence of the bulk current. Furthermore, the deviation of the I_D-V_G plot from the linear relationship is found in Fig. 3(b). This shows the possibility that the Dy@C_{82} FET operates as enhancement-type when the bulk current vanishes. Consequently, the normally-on character of this FET can be explained by the fact that the E_g for Dy@C_{82} thin-film, 0.2 eV, is smaller by one-order than those for C_{60}, 1.8 eV [14,18]. Furthermore, the UPS spectrum shows the E_g of 0.35 eV for La@C_{82} [19]. Thus three-electron transfer in Dy@C_{82} and La@C_{82} lead to small-gap semiconducting behavior, instead of metallic behavior, probably as a result of strong electron correlation in metallofullerenes. Therefore, the normally-on FET character should be caused by the bulk current based on the small-gap semiconducting property of Dy@C_{82}. Very recently, n-channel normally-on type FET characteristics were confirmed for $La_2@C_{80}$ [20], as in the Dy@C_{82} FET. The μ for the $La_2@C_{80}$ FET was as low as that of the Dy@C_{82} FET. The low μ in the $La_2@C_{80}$ FET was mainly attributed to the low crystallinity of the thin film. This implies that the metallofullerene FETs urgently require the techniques for fabricating thin films of metallofullerenes with high crystallinity.

3.3. *Transport properties of C_{60} FET*

The information on the transport property of the C_{60} FET is important for controlling physical properties through the field-effect carrier doping to C_{60}. The μ *vs.* temperature plot in the C_{60} FET is shown in Fig. 4(a). The C_{60} FET used differs from those described in 3.1, where the μ value is higher than that observed here, 1.8 x 10^{-2} cm^2 V^{-1} s^{-1} at 295 K. The μ increases monotonically with increasing temperature up to 300 K. The FET characteristics cannot be observed below 220 K. The plot of ln μ vs. the inverse temperature, shown in the inset of Fig. 4(a), exhibits a linear relationship. This suggests hopping transport for the conduction mechanism of the C_{60} FET. The activation energy E_a is estimated to be 0.29 eV. We can point out from this observation that the transport of C_{60} FET follows the hopping mechanism found in the pentacene FET with μ=0.3 cm^2 V^{-1} s^{-1} [9]. On the other hand, the pentacene FET with μ as high as 1.5 cm^2 V^{-1} s^{-1} showed a temperature-independent μ [9]. These results imply that the transport mechanism changes with increasing $\tilde{\mu}$ Therefore the temperature dependence of μ shown in Fig. 4(a) is the transport property appearing in the region of $\mu = 10^{-3} - 10^{-2}$ cm^2 V^{-1} s^{-1}. In the temperature dependence of V_T for the C_{60} FET, shown in Fig. 4(b), the V_T decreases with increasing temperature. The origin cannot clearly be explained.

3.4. CMOS inverter with fullerene and pentacene FETs

We have fabricated a CMOS logic NOT circuit composed of an n-channel FET and a p-channel FET. The structure of CMOS inverter circuit is shown in Fig. 1(b). The gates of the n- and p-channel FETs are connected, and they serve as an input node (V_{in}). The drains of the two FETs are also connected, and they serve as an output node (V_{out}). The source of the n-channel FET is grounded, while the source of the p-channel FET is connected to a power supply ($V_{DD} > 0$), where V_{DD}=70 V was applied in the present study.

The drain currents, I_{Dn} and I_{Dp}, for the C_{60} (n-channel) and pentacene (p-channel) thin-film FETs were measured as a function of V_{out}, where the drain-source voltage for the n-channel FET, V_{DS}, and the source-drain voltage of p-channel FET, V_{SD}, correspond to V_{out}

and $V_{DD} - V_{out}$, respectively. The intercepts of I_{Dn} and I_{Dp} represent the steady-state operation points of the CMOS inverter. The plot of V_{out}-V_{in} estimated from the intercepts, shown in Fig. 5(a), corresponds to the transfer characteristics of this circuit. The V_{out}-V_{in} plot shows a clear characteristic of the CMOS inverter. The plot of V_{out}-V_{in} measured directly in the circuit is shown in Fig. 5(b); the threshold voltage of this circuit, V_{TIC}, is $\approx$25 V. This plot is consistent with the V_{out}-V_{in} plot shown in Fig. 5(a), supporting that this circuit operates as an inverter with the voltage gain of 4.0. This is the first logic gate circuit with fullerene FET.

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