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Description	

Silicon on insulator for symmetry-converted growth

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Integration of metals and semiconductors having three- or sixfold symmetry on device-oriented [i.e., (001)] silicon wafers, which have fourfold symmetry, has been a long-standing challenge. The authors demonstrate that, by using symmetry-converted (111) silicon on insulator, wurtzite-structure gallium nitride, which has threefold symmetry, can be integrated with Si(001). The stability of the symmetry-converted Si(111) layer makes this technique appealing to the commercial integration of wide-ranging important materials onto Si(001) base wafers. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2748099]

Silicon serves as the fundamental material for the semiconductor industry because of its superior processability in the fabrication of various device structures and especially because of its ability to form a high-quality oxide. Si(001), with a square surface lattice, has been used for actual device fabrication primarily because of the lower interface state density. A major and important class of materials having three- or sixfold symmetries has intrinsic difficulty growing on Si(001) because the symmetry mismatch at the interface induces polycrystalline-film formation and roughness, factors that seriously degrade electronic and optoelectronic performances. For this reason, many important and interesting systems, such as Pb quantum wells, where the quantum size effect controls superconductivity,[1] organic network structures,[2] and GaN films[3–6] with promising applications for optoelectronics and power devices, have been studied using Si(111) substrates, thus at least avoiding the symmetry mismatch issue. However, the use of Si substrates with indices other than (001) in technology has been limited by the poor quality of oxide/Si interface mentioned above.

In this letter, we present a general solution for this long-standing problem by utilizing a silicon-on-insulator (SOI) structure where a thin Si(111) layer is bonded to Si(001) via the oxide layer. We can thus use the Si(111) template layer in those regions where we need to integrate a three- or sixfold symmetric material, while using the Si(001) wafer in other regions to create complementary metal oxide semiconductor electronic devices. This SOI structure provides a uniform Si(111)-7×7 clean surface using the surface treating method recently developed for the Si(001)-SOI surface.[7] The thin Si layer with the clean surface is stable up to 800 °C, enabling the growth of a broad range of materials tested previously on Si(111)-7×7. A GaN film is directly grown on this SOI structure to demonstrate the validity of our approach. The ultrathin Si(111) layer, with a thickness of 14 nm, is stable against the irradiation of Ga- and N-plasma fluxes at the

growth temperature, which results in the formation of uniform N-polar GaN film on the SOI structure.

A SOI wafer with a 100 nm thick Si(111) template layer and 200 nm thick oxide layer on a Si(001) handle wafer, fabricated by the Smart Cut™ technique, was obtained from SOITEC. The Si(111) layer has a resistance of 13–22 Ω cm. This layer was oxidized at 1100 °C for 80 min. The oxidized surface layer was removed by HF to leave 14 nm of unoxidized Si(111), as measured using ellipsometry. This SOI (Fig. 1) was used for the present work. The *ex situ* cleaning of the sample was achieved by treating it in HCl and H_2O_2 solutions (HCl (35% aq.):H_2O_2 (30% aq.):purified water =4:5:5) at 80 °C for 10 min twice, removing surface oxide with 5% HF solution after the first treatment. The thickness decrease by this treatment is estimated as 1 nm or less, which is the typical thickness of the native-oxide layer. The specimen was loaded in an ultrahigh vacuum molecular beam epitaxy–scanning probe microscope (UHV MBE-SPM) system, which consists of three UHV chambers (SPM, photoemission, and MBE) with base pressures better than 1.0×10^{-8} Pa and an additional high-vacuum load-lock chamber. After a degas at 600 °C for 12 h, 1 ML/min of Si flux from a resistively heated Si wafer was applied for 5 min to the specimen surface held at 750 °C to remove the surface oxide layer that had built up during the transfer and degas. Finally, the specimen was annealed at 800 °C for 2 min to obtain the Si(111)-7×7 reconstruction. GaN was grown following the method described in Ref. 5. The SOI substrate is nitrided by a N plasma (rf power: 300 W, N_2 pressure: 2 $\times 10^{-3}$ Pa) at substrate temperature of 700 °C for 3 min to form a silicon nitride layer prior to the growth. After that, the N-plasma condition is set at rf power of 300 W and N_2 pressure of 3×10^{-3} Pa for the growth. GaN is nucleated and grown at a fixed substrate temperature of 750 °C, and the Ga K-cell temperature is kept at 980 °C for the nucleation layer growth, to give a relatively lower beam equivalent pressure (BEP) of 1.3×10^{-4} Pa at the Ga flux monitor. These parameters assure a N-rich condition to allow uniform N-polar nucleation at the initial growth stage.[5] After 10–20 min of nucleation layer growth, the K-cell temperature is increased

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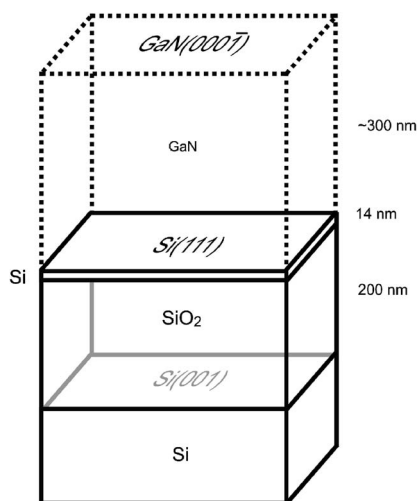a)Electronic mail: fujika-0@imr.tohoku.ac.jp

FIG. 1. Schematic diagram of the SOI structure used for GaN growth. A thin Si(111) template layer is bonded with a Si(001) substrate via SiO$_2$ layer, converting the substrate symmetry from square to hexagonal.
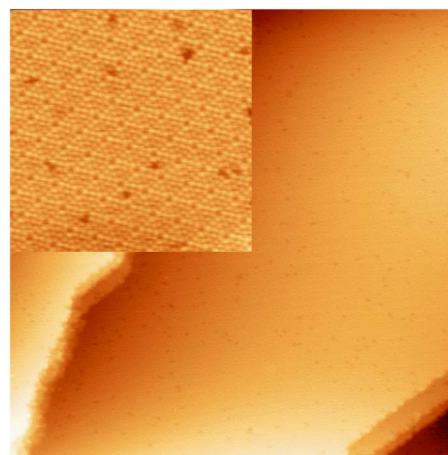

FIG. 2. (Color online) STM images of the Si(111)-7×7 reconstructed surface on the SOI structure, obtained by the Si deposition cleaning method. Sample bias voltage is set at −1.0 V (inset: +1.3 V), and scan size is 100 × 100 nm^2 (inset: 25×25 nm^2).

to 1050 °C (BEP: 3.5×10^{-4} Pa) to change the growth condition to a Ga-rich one, in order to grow a flat GaN film.[5] All growth processes are monitored in real time by reflection high-energy electron diffraction (RHEED). GaN films approximately 300 nm thick were grown.

Scanning tunneling microscopy (STM) observations are carried out with a W tip installed in the JEOL-4500A SPM head at a tunneling current of 30 pA. The STM tip is located at the center of the specimen, which has a width of 1.2 mm and a 3 mm gap at its center, between tantalum sheet clamps at both ends.

Figure 2 shows STM images of the symmetry-converted SOI surface prepared by cleaning with *in situ* Si deposition and successive annealing. A uniform surface with flat terraces is observed, accompanied by typical Si(111)-7×7 atomic structures. The Si(001)-2×1 dimer-row structure can be observed after flash heating this specimen at 1350 °C (not shown). At this temperature, the oxide decomposes and the Si(111) template layer will disappear with it. The fact that we observe first the clean-Si(111) surface structure and later, after oxide decomposition, the Si(001) surface structure confirms that the surface Si(111) layer was bonded to Si(001). The stable tunneling current to the thin Si(111) layer assures that the Si(111) template layer, which is the only possible source of the conductivity on the insulating oxide layer, maintains connectivity to the end of the specimen even after the surface treatment. Resistance measurements of the point contact of the STM tip to the sample surface give stable values in the range of 10^7 Ω. Because point contacts to bulk-Si(111) surfaces always give resistances of 10^6 Ω or less, the higher resistance measured for the thin template layer of SOI(111)/Si(001) must be dominated by the sheet resistance of the Si(111) template layer with its clean-Si(111) surface. The carrier density in the 14 nm Si(111) template layer is estimated to be 10^{15} cm^{-3} from the resistance of the original wafer,[8] giving an areal density of 10^9 cm^{-2} in the Si(111) template layer. This density is much smaller than the adatom density on the Si(111)-7×7 surface (10^{14} cm^{-2}) or the oxide/Si(111) interface trap density [$10^{11}-10^{12}$/cm^2 eV for the Si(111)/SiO$_2$ interface, distributed uniformly across the 1.1 eV wide band gap[8]]. Therefore, with this thickness of template layer, the carriers in the bulk band are totally

depleted[7] because it is known that the Si(111)-7×7 surface pins the Fermi level almost exactly at the middle of the band gap.[9] Therefore, the charge carrier transport through the thin Si(111) membrane observed here, which enables the STM observation, cannot be via conventional bulk conduction but must be via the Si(111) surface state bands directly.

The resistance of the same SOI surface increases to 10^{10} Ω by depositing a fraction of a monolayer of Ga to form the Si(111)-$\sqrt{3} \times \sqrt{3}$-Ga reconstruction. This reconstruction eliminates the in-gap surface bands of the clean surface[10] and thus eliminates the surface conduction channel. This resistance change is completely reversible with the removal of Ga at 750 °C, a result that allows us to exclude the possibilities of permanent changes in morphology and doping status. The observations above strongly support our conclusion on the mechanism of conduction in these films.

GaN is grown on this well-defined Si(111)-7×7 reconstructed structure. RHEED observations of the clean substrate [Fig. 3(a)] give a 7×7 streak pattern with no evidence of possible agglomeration of Si three-dimensional islands in
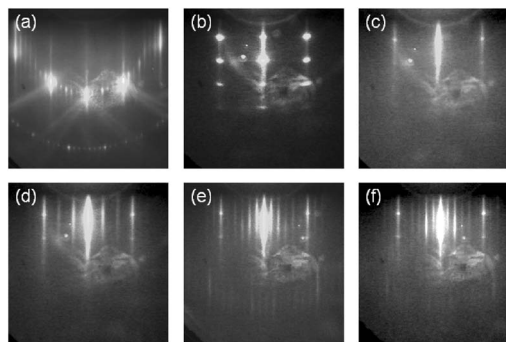

FIG. 3. (Upper row) Sequential change of RHEED patterns during the growth of GaN films on symmetry-converted SOI, observed with an electron beam parallel to Si⟨1$\bar{1}$0⟩ showing (a) the 7×7 reconstruction of the SOI(111) surface, (b) nucleation of wurtzite GaN, and (c) after film growth. (Lower row) Sequential change of surface reconstruction with the deposition of additional Ga on the GaN film at room temperature observed with an electron beam parallel to GaN⟨$\bar{1}\bar{1}$20⟩, which aligns to Si⟨1$\bar{1}$0⟩. The patterns correspond to GaN(000$\bar{1}$)-(d) 3×3, (e) 6×6, and (f) c(6×12) reconstructions with higher intensity in three time streaks, which are all known for the N-polar GaN surface.

the Si(111) template layer (spots in the RHEED pattern) before growth. Initial nitridation gives a diffuse RHEED pattern, indicating the existence of a disordered nitride layer on the surface.[5] Because the initial nucleation is performed under N-rich conditions to allow initial N-polar nucleation,[5] the lack of a Ga surfactant effect[11] causes the growth to proceed in the three-dimensional mode. At this nucleation stage of GaN, we obtain a RHEED pattern [Fig. 3(b)] consisting of transmission diffraction spots, without any streaky component from possible regions of flat growth. From this transmission RHEED pattern, GaN is determined to be wurtzitic, having the following epitaxial relationship with the Si(111) layer: GaN $\langle 0001 \rangle \| Si \langle 111 \rangle$ and GaN $\langle \bar{1}\bar{1}20 \rangle \| Si \langle 1\bar{1}0 \rangle$, similar to earlier results on conventional bulk Si(111).[5] After changing the growth condition to a Ga-rich one, the RHEED pattern recovers its streaky nature [Fig. 3(c)], indicating improvement to a smoother surface morphology under these conditions. The GaN in-plane lattice constant, derived from the RHEED analysis, is 0.319 ± 0.002 nm. This value, close to that of pure GaN, suggests that the lattice mismatch stress between the GaN film and Si(111) is mostly relaxed via the generation of dislocations, within experimental error.

GaN surfaces are known to exhibit prominent reconstructed features upon the deposition of Ga, depending on the film polarity.[12] Ga deposition on the GaN film formed on the SOI(111) structure results in clear and high-intensity 3×3, 6×6, and $c(6 \times 12)$ RHEED patterns [Figs. 3(d)–3(f)], depending on the amount of Ga deposited on the 1×1 surface, which are typical of the N-polar film.[12] STM observations of these Ga covered surfaces demonstrate uniform imaging of atomically resolved features (Fig. 4), which has been reported for N-polar reconstructions.[12] Antipolar domains, typically covered by a Ga-fluid surface after Ga termination,[5] were never found in our observations, confirming that N-polar GaN was selectively grown on the SOI(111) surface. Even at the end of the growth, the conductivity of the SOI structure was not damaged.

The growth of GaN on conventional SOI(001) (Ref. 13) and conventional SOI(111) (Ref. 14) [template and handle wafer both Si(111) and also a much larger template layer thickness] has been investigated with the goal of enhancing strain relaxation between the GaN and the Si. The improved relaxation of residual strain in a thick GaN layer has already been reported on a 200 nm thick (111) SOI layer without symmetry conversion.[14] The stability of ultrathin SOI(111) layers down to at least 10 nm widens the application of this symmetry conversion technique by allowing the completion of strain relaxation in an earlier stage of growth.

The wurtzite GaN growth on symmetry-converted SOI with a (001) handle and a (111) oriented template layer, shown in this letter, has potential technological importance by enabling integrated GaN devices intermingled with Si controlling circuits on a single chip. Direct growth of single-domain wurtzite GaN on vicinal Si(001) via an AlN seed layer[15] aims at the same goal. The growth of GaN on SOI reported here will be more suitable for integration of GaN with Si devices because it is possible to avoid direct contact of other elements with Si(001) and there is no need for a large miscut angle of the Si(001) substrate. The Si(111) template layer is stable under a nitrogen flux for nitridation and a Ga flux for successive growths at temperatures between 700 and 800 °C. This stability of a thin Si(111) layer on the
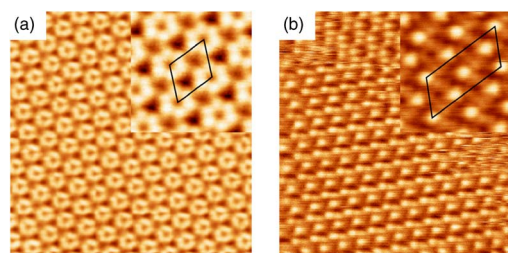

FIG. 4. (Color online) STM images of the GaN(000$\bar{1}$)- (a) 6×6 and (b) $c(6 \times 12)$ reconstructed surfaces obtained by Ga deposition on the GaN films grown on the SOI structure. Scan size is 20×20 nm^2. Insets are the magnified images (5×5 nm^2). Sample bias voltages are set at (a) +1.1 V (inset: −0.9 V) and (b) +1.1 V (inset: −1.0 V). A phase boundary originating from rotated reconstruction is seen in the upper part of the $c(6 \times 12)$ image.

SOI structure enables most of the heteroepitaxial growths reported on Si(111)-7×7 that can be performed at lower growth temperatures. The stability of the orientation converted SOI membrane on Si(001) observed here would enable general integration of the intriguing class of materials with three- or sixfold surface symmetries,[1,2] as well as functional high-index surfaces,[16] with Si devices.

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