[See page 312 for Figure 4/Table 1.]

SESSION III: DIGITAL GaAs CIRCUITS

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WAM 3.1: A 1K-Gate GaAs Gate Array*

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TO ACHIEVE the high-speed capability of GaAs ICs, it is desirable to integrate more and more logics in a single chip. The gate array approach is effective for GaAs as well as for Si ICs in enabling logic designers to obtain the logic functions relatively easily. To date, GaAs gate arrays with hundreds of gates in a chip have been reported[1-4]. This paper will report on the fabrication of 1K-gate GaAs gate arrays with DCFL (Direct Coupled FET Logic) circuitry using a Pt-buried gate process[5,6] Application of this technology to a 6x6b parallel multiplier and its complete operation will also be described.

A photomicrograph of the gate array is shown in Figure 1. The chip size of the gate array is 3.75mm x 3.75mm. Shown in Figure 2 are the layout and the equivalent circuit representation of the basic cell, which measures 34μm x 75μm and can be programmed as a DCFL 3-INPUT NOR gate. The gate width/length are 10/1 (microns) for the DFET load and 20/1 for EFET drivers. There are 14 columns and each column has 75 basic cells, totaling 1050 gates in a chip. Between the columns, there are 13 interconnection tracks whose width is 108μm. The design rules of 2μm line width, 3μm line spacing and 2μm x 2μm contact hole allow 13 1st-level interconnection lines to run in each track parallel to the column direction. The 2nd-level interconnection lines (3μm wide and 4μm spacing) can run across the column with the restriction that they should not run above the FET gate region. The power supply was designed carefully with the layouts of the (VDD) 1st-level and ground (GND) 2nd-level lines to avoid low noise margin problems associated with DCFL circuitry. Surrounding the array region are the VDD and GND main lines, 56 I/O buffers and pads. The circuit used for I/O buffers is shown in Figure 3. It occupies a 110μm x 120μm area adjacent to a pad. Input buffers are DCFL power inverters. Output buffers available include EFET open drain circuits for TTL interfaces, DFET source followers for ECL interfaces, DCFL power inverters and EFET push-pull circuits. A specific buffer was selected by the interconnection layout mask for each interfacing purpose.

Propagation delay time (tpd) dependence on the interconnection line depth (L), the number of fanouts (Nf) and crossovers was evaluated by measuring ring oscillators with various loads at VDD=1 V. The results obtained are as follows. The unloaded gate delay time was 100ps/gate and the delay time increased at a rate of 65ps/mm, 27ps/fanout and 3.33ps/crossover at 0.2mW/gate power dissipation. This leads to a tpd=350ps/gate under the loading condition of L=3mm and Nf = 3. The features of the gate array are summarized in Table 1.

This gate array has been applied to a 6 x 6b parallel multiplier circuit employing a *carry save* algorithm and is illustrated in Figure 4. The fabricated circuit is shown in Figure 1. It consists of 379 internal gates, occupying approximately 70% of the array area in the actual layout. Output buffers selected were DCFL power inverters followed by EFET push-pull circuits. An example of the low frequency test results with high load impedance is shown in Figure 5. Complete operation with satisfactory output logic swings was confirmed. High-speed testing was also performed directly on the wafer using a probe card modified and calibrated for a 50-ohm system. Figure 6 shows the input and output waveforms indicating the responses for the critical path and the most significant output bit (P11). The multiplication time measured on these waveforms was 10.6ns, whereas the total chip power consumption was 380mW, including input and output buffering operation. The output logic swing obtained was about 200mV when driving the off-chip 50-ohm system and about 1V for high load impedances, which is enough to drive other GaAs DCFL inputs.

Acknowledgments

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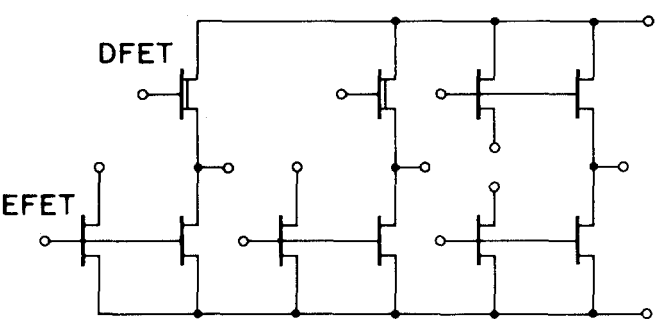

FIGURE 3—I/O buffer circuitry.

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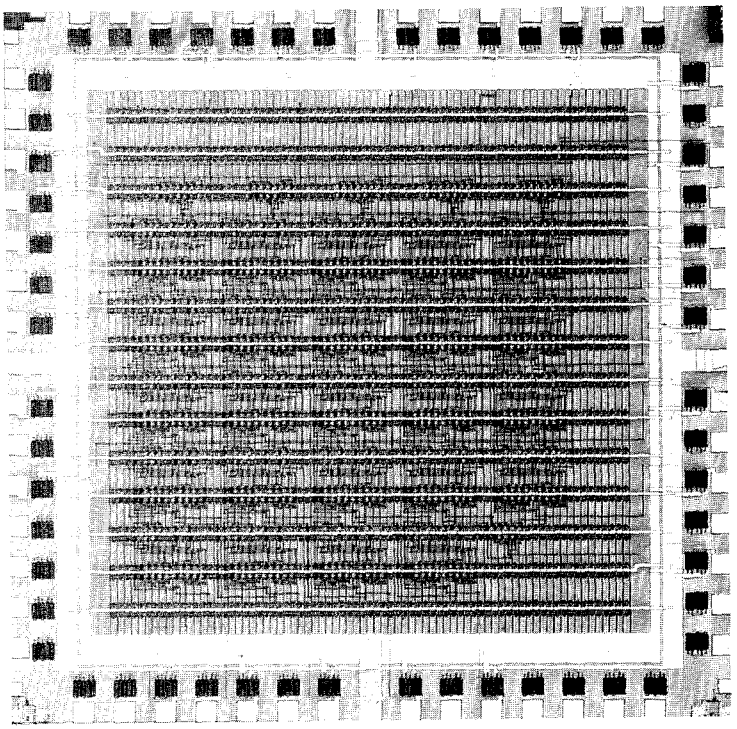

[Left]

FIGURE 1—Photomicrograph of 1K-gate GaAs DCFL gate array chip used in 6x6b parallel multiplier.

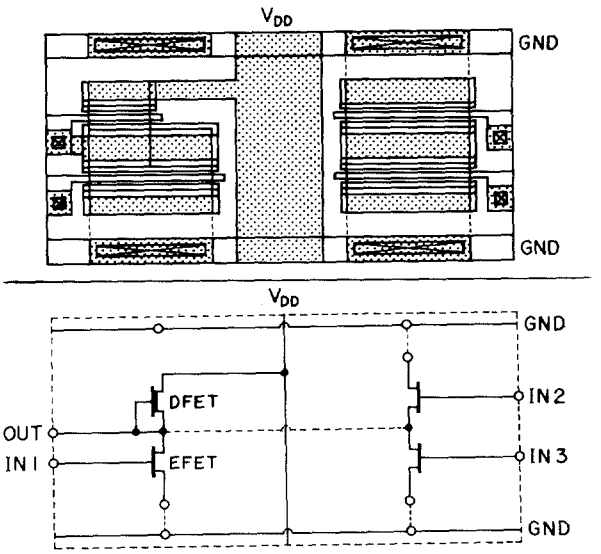

FIGURE 2—Basic cell layout and corresponding circuit representation.

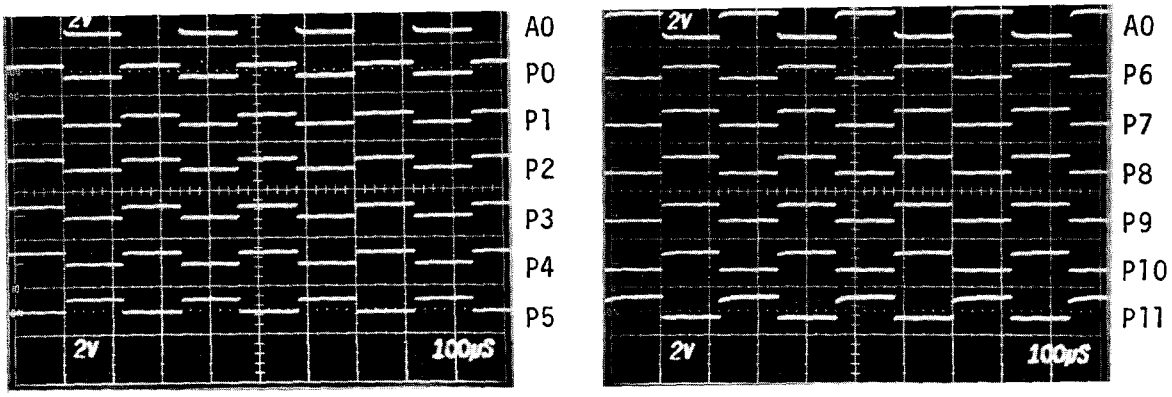

FIGURE 5—Outputs of 6x6b parallel multiplier at low frequency test. The input code is 10000S x 111111 = SSSSSSSSSSSS, where S is sequential 0/1 pulse applied to A0. VDD = 1.5V, P = 380mW.

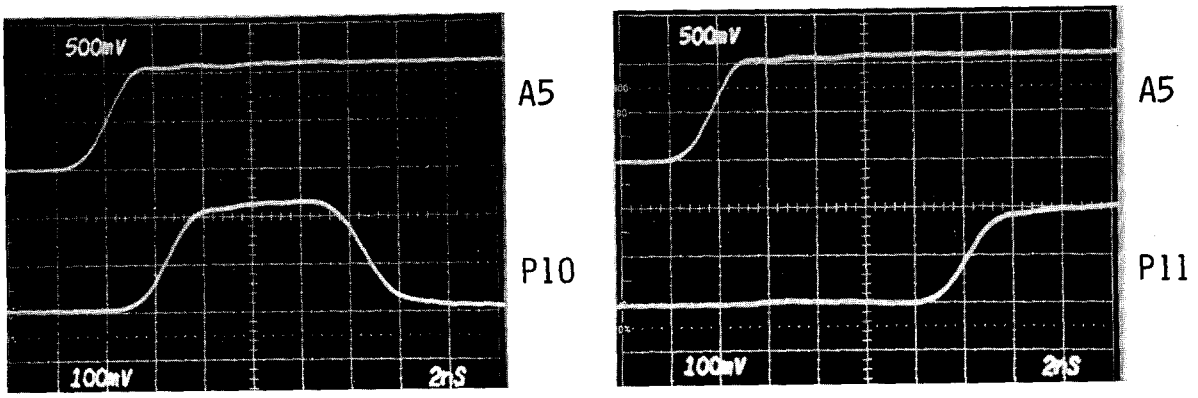

FIGURE 6—Output waveforms of product bits P10 and P11 when S00001 x 111111 = S000005̄11111 multiplication was performed, S is the pulse applied to A5 which changes from 0 to 1 state. At first, output P10 rises, responding to fast arrival of A5B5 (=1) calculation at FA24. It then returns to zero as result of carry signal from FA23 to FA24. This corresponds to the critical path of multiplier. VDD = 1.5V, P = 380mW.

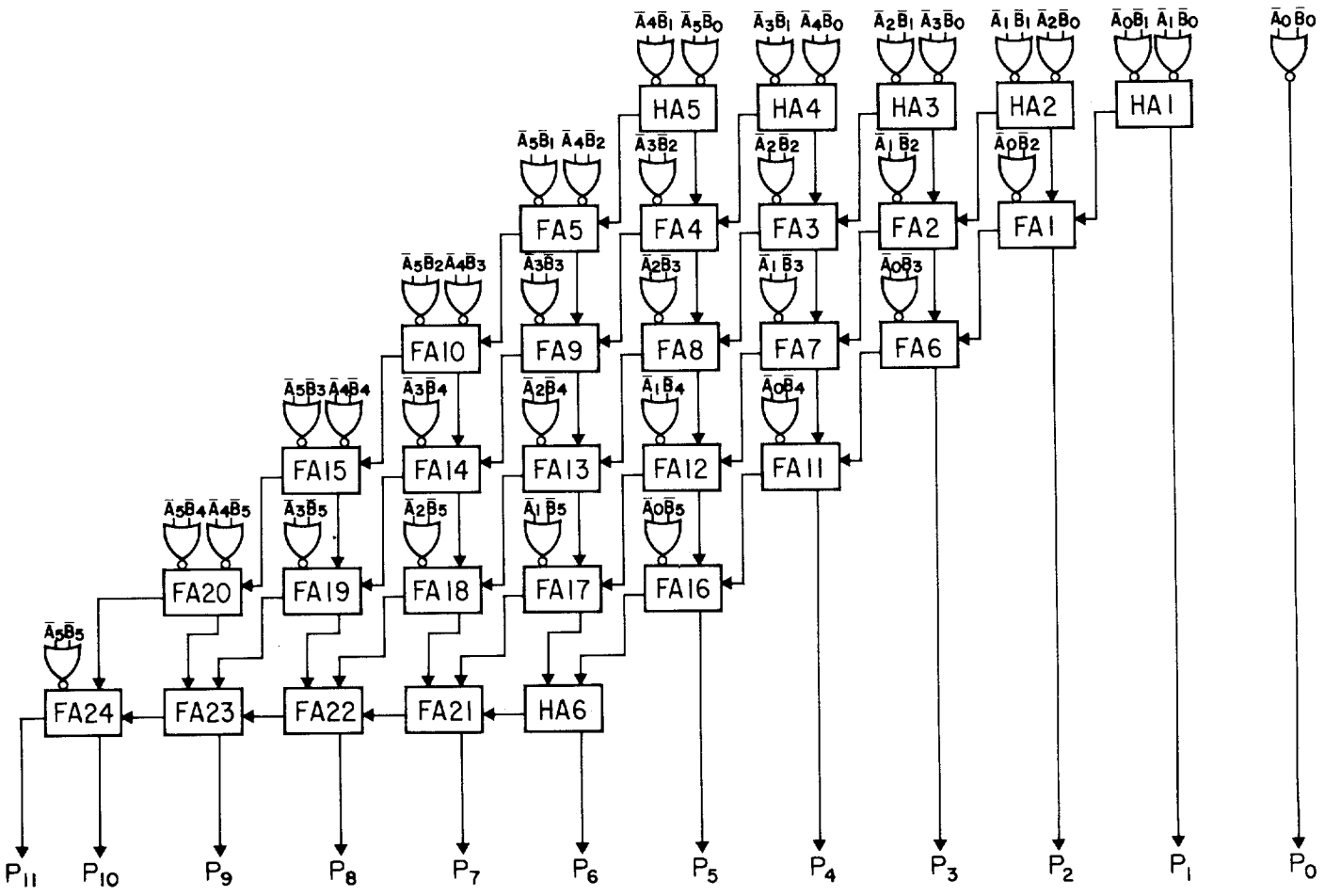

FIGURE 4—Block diagram of 6x6b parallel multiplier using *carry save* algorithm.

TABLE 1—Performance of 1K-gate GaAs DCFL gate array.

Chip size	3.75 mm x 3.75 mm
Basic cell	3-INPUT NOR (DCFL)
FET size (mask)	10/1 (μm) DFET load 20/1 (μm) EFET driver
FET source-drain spacing	2 μm (n^+-source, drain)
Design rule of interconnection	
1st level	2-μm wide, 3-μm spacing
2nd level	3-μm wide, 4-μm spacing
contact hole	2μm x 2μm
FET performance measured	
g_m	110 mS/mm
V_{th}	0.1 V(EFET), -0.7 V(DFET)
L_g (gate length)	1.0 μm
Propagation delay time unloaded (fan-out=1)	100 ps/gate
power level	0.2 mW/gate
dependence on load	27 ps/fan-out 65 ps/mm 3.33 ps/cross-over
Propagation delay time under loading condition of L=3mm, Fan-out=3	350 ps/gate (0.2 mW/gate)