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Author(s)	Toyoda, Nobuyuki; Uchitomi, Naotaka; Kitaura, Yoshiaki; Mochizuki, Masao; Kanazawa, Katsue; Terada, Toshiyuki; Ikawa, Yasuo; Hojo, Akimichi
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SESSION XV: HIGH SPEED ARRAYS

THPM 15.6: A 42ps 2K-Gate GaAs Gate Array*

Nobuyuki Toyoda, Naotaka Uchitomi, Yoshiaki Kitaura, Masao Mochizuki, Katsue Kanazawa, Toshiyuki Terada, Yasuo Ikawa, Akimichi Hojo

Toshiba VLSI Research Center

Kawasaki, Japan

TO INCREASE speed of microelectronic systems, it is the interchip signal delay that should be reduced by maximizing the integration level. As the integration level increases, however, the development time becomes longer. The rapid development of LSIs is increasingly important because the product life cycle has been becoming shorter. A gate array approach is effective under these circumstances. Very high-speed ICs such as Si bipolar ECL logic, is no exception, and 2.5-5.0K gate gate arrays with 0.35-0.50ns loaded gate delay have been developed. However, very large power consumption, 5-8W/chip, limit their field of application. GaAs gate arrays have attracted interest as a replacement for the Si ECL gate array because of the smaller gate delay and lower power consumption. To date, several types of GaAs gate array have been reported[1,2,3]. This paper will describe a 2K-gate DCFL (Direct Coupled FET Logic) GaAs gate array with a 42ps unloaded and 215ps loaded gate delay at a power dissipation of 0.5mW/gate. An 8 x 8b parallel multiplier has been fabricated on this chip. A multiplication time of 8.5ns was achieved at a power dissipation of 400mW, an improvement over an 8 x 8b Si ECL multiplier with custom design[4]. The current design also consumes about 35% less power.

Figure 1 shows a photomicrograph of the chip, in which 112 row x 18 column (= 2016) basic logic cells, 66 I/O buffer cells and 77 pads are included. Chip size is 4.59mm x 4.73mm. One basic cell (84μ x 24μ) consists of three EFETs (W_g/L_g = $20/1.5\mu$) and one DFET (W_g/L_g = $10/1.5\mu$) with 5μ wide V_{dd} and GND lines. Each cell can be personalized as an inverter, or a 2- or 3-INPUT NOR gate. Figure 2 shows a photomicrograph of a part of a personalized chip. Between columns, 15 interconnection tracks are prepared for 2μ wide 1st-level interconnection lines with 3μ spacings. Three 2nd-level interconnection lines with the design rule of 3μ width and 4μ spacing can run over each basic cell. The minimum size of contact hole is 2μ x 2μ. The power supply and ground lines have been designed so that the V_{dd} voltage drop or the GND voltage rise should never exceed 50mV. Input and output buffers are implemented with large (W_g/L_g = $200/1.5\mu$ for EFET, W_g/L_g = $100/1.5\mu$ for DFET) DCFL push-pull circuits.

The gate array was fabricated with WN gate self-aligned MESFET process technology. WN has lower resistivity ($70\mu\Omega$) and a larger Schottky barrier height (0.84V) to GaAs in comparison with other refractory metals such as TiW and WSi, and is therefore most suitable for DCFL circuitry. Active layers for E- and D-FETs were formed by Si ion implantation at 50KeV and successive capless annealing at 850°C for 15 min. The WN gate metal was deposited by reactive RF sputtering in Ar + N_2 mixed gas. The average threshold voltages were +0.21V for EFET and −0.47V for DFET. The 1st and 2nd interconnection lines were Ti/Pt/Au.

To evaluate gate performances, five types of ring oscillators were fabricated. Table 1 summarizes the propagation delay times under various loading conditions at V_{dd} = 1V. From these experimental data, the increments of delay time due to fan-in, fan-out, interconnection line and crossover capacitances, were calculated and are shown in Table 2. If the average loading condition is postulated to be fan-in = 3, fan-out = 3, interconnection line length = 2mm, which is a similar or slightly heavier loading condition than is usual for Si ECL or CMOS gate array, the loaded delay time becomes 215ps, when the power dissipation is 0.5mW/gate.

An 8 x 8b parallel multiplier and a full adder ring oscillator were also fabricated on the same gate array chip. Figure 3 shows the schematic logic diagram of a multiplier circuit employing a carry save algorithm. It consists of 8 half adders (HA), 48 full adders (FA), 64 NOR gates and 32 I/O buffers. 728 basic cells were used and approximately 50% of gate array area was occupied. The maximum multiplication time is obtained when the partial product, A_7B_0, propagates through the critical path to P_{14} as shown in Figure 3. Therefore, high-speed testing was performed on the wafer, which had passed the low frequency functional testing, with input code A = S0000001 and B = 11111111. Figure 4 shows the input pulse applied to A_7 and the output waveforms which appeared at P_7 and P_{14}. The delay times were 4.4ns and 8.5ns, respectively, whereas the power dissipation was 228mW for an 8 x 8b parallel multiplier and 176mW for I/O buffers at V_{dd} = 1.4V.

The delay time at each product bit, P_i, can be predicted by using the data obtained from a full adder ring oscillator. Figure 5 shows the schematic logic diagram of a 6-stage full adder ring oscillator and the full adder logic circuit. From the "B = 0, C = 0" mode ring oscillation, the propagation delay time when signal passes through two NOR gates in a full adder is experimentally obtained. The *carry* signal propagation delay time, t_c^{FA}, is almost equivalent to this time. The *sum* signal propaga-

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[1] Toyoda, N., et. al., "500 Gates GaAs Gate Array", *Solid-State Devices Conference, Digest of Technical Papers*, Tokyo, p. 187; Aug., 1982.

[2] Ikawa, Y., et. al., "A 1K-gate GaAs Gate Array", *ISSCC DIGEST OF TECHNICAL PAPERS*, p. 40; Feb., 1984.

[3] Yuan, H., et. al., "GaAs Heterojunction Bipolar 1K Gate Array", *ISSCC DIGEST OF TECHNICAL PAPERS*, p. 42; Feb., 1984.

[4] Yamauchi, H., et. al., "10ns 8 x 8 Multiplier LSI Using Self-Align Process Technology", *IEEE J. Solid-State Circuits*, Vol. SC-18, No. 2; April, 1983.

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tion delay time, t_s^{FA}, is obtained directly from the "B = 1, C = 0" mode ring oscillation. The experimental values were t_c^{FA} = 540ps and t_s^{FA} = 670ps. The response time at P_7 and P_{14} product bits for S0000001 x 11111111 multiplication were calculated from the following equations;

$$t_{P7} = t_{NOR} + t_s^{HA} + 6t_s^{FA} + 2t_{BUF} \approx 7t_s^{FA}$$

$$t_{P14} = t_{NOR} + (t_s^{HA} + t_c^{HA}) + 6(t_s^{FA} + t_c^{FA}) + 2t_{BUF}$$

$$\approx 7(t_s^{FA} + t_c^{FA})$$

where t_{NOR}: NOR gate delay time, t_s^{HA}, t_c^{HA}: sum and carry delay times in a half adder, t_{BUF}: I/O buffer delay. The calculated values of t_{P7} and t_{P14} were 4.7ns and 8.6ns, which consistently agreed with the directly measured values shown in Figure 4.

Acknowledgments

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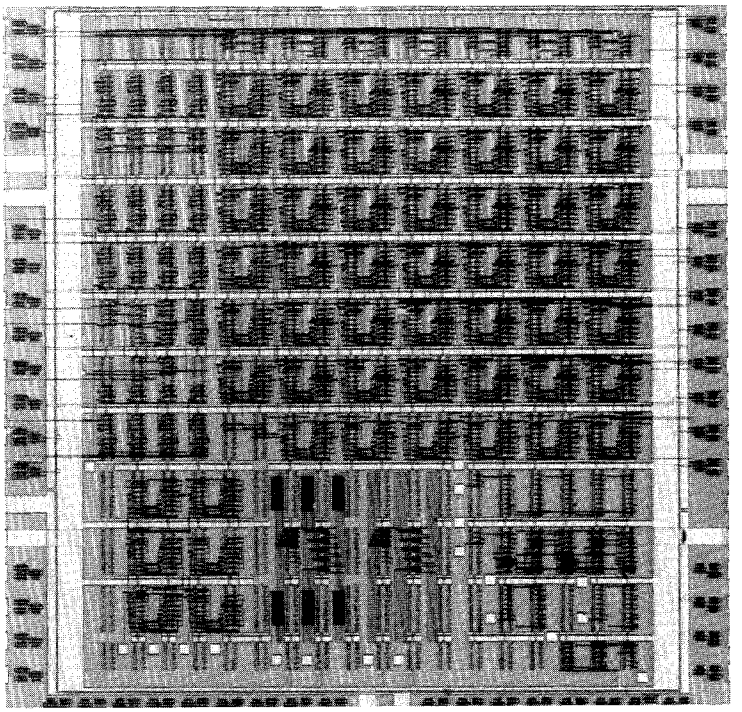

FIGURE 1—Photomicrograph of 2K gate GaAs gate array on which five types of ring oscillators, a full adder ring oscillator and an 8 x 8b parallel multiplier were fabricated.

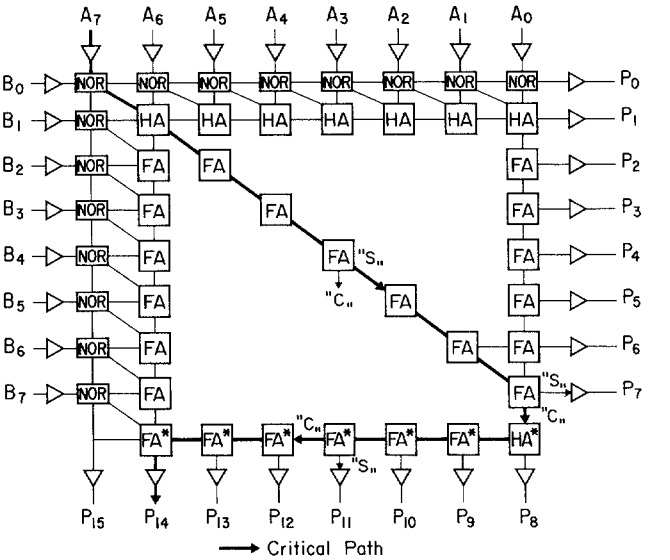

FIGURE 3—Logic diagram of an 8 x 8b parallel multiplier. NOR = NOR gate, FA = full adder with NOR gate, FA* = full adder, HA = half adder with NOR gate, HA* = half adder. *S* is *sum* signal and *C* is *carry* signal.

Loading Conditions	tpd (ps)
FI=1 FO=1	42
FI=1 FO=3	75
FI=3 FO=1	63
FI=1 FO=1 L=2mm	155
FI=1 FO=1 L=2mm CO=100	255

Pd = 0.5mW/gate

TABLE 1—Propagation delay times under various loaded conditions, where "C.0-100" means that the 2mm-long 1st level interconnection line crosses over the gounded 2nd level interconnection line 100 times between each inverter.

Δt_{pd}/F.I.	11	ps/F.I.
Δt_{pd}/F.O.	16	ps/F.O.
Δt_{pd}/LINE	59	ps/mm
Δt_{pd}/C.O.	0.95	ps/C.O.

Pd = 0.5mW/gate

TABLE 2—Delay time increments due to fan-in, fan-out, interconnection line and crossover capacitances.

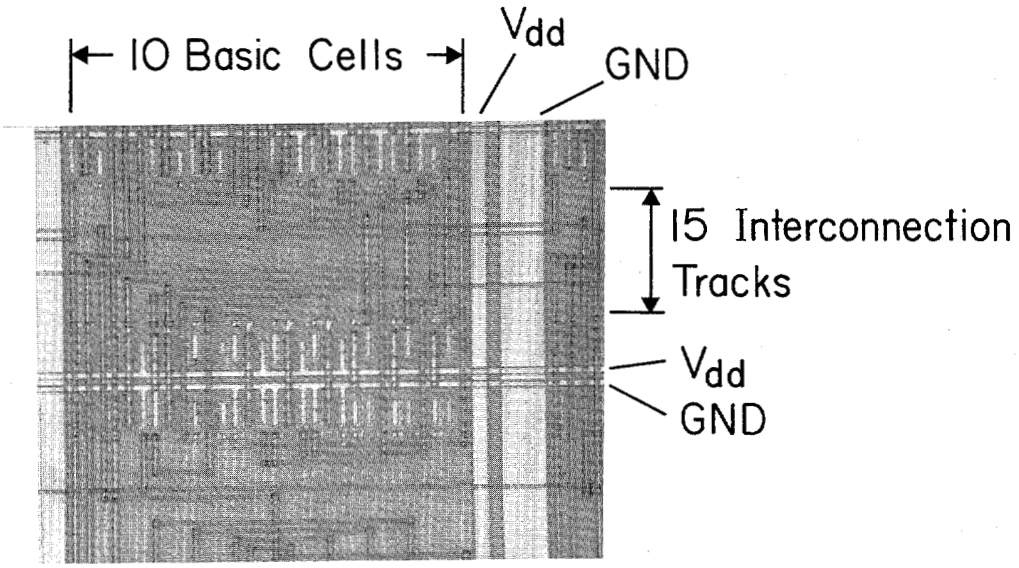

FIGURE 2—Part of gate array after being personalized.

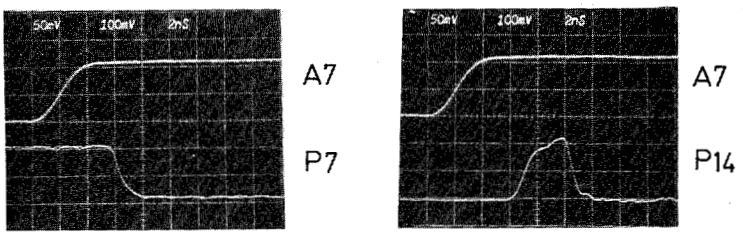

FIGURE 4—Input pulse (S) applied to A_7 and output waveforms at P_7 and P_{14} when A(= S0000001) x B(= 11111111) multiplication was performed.

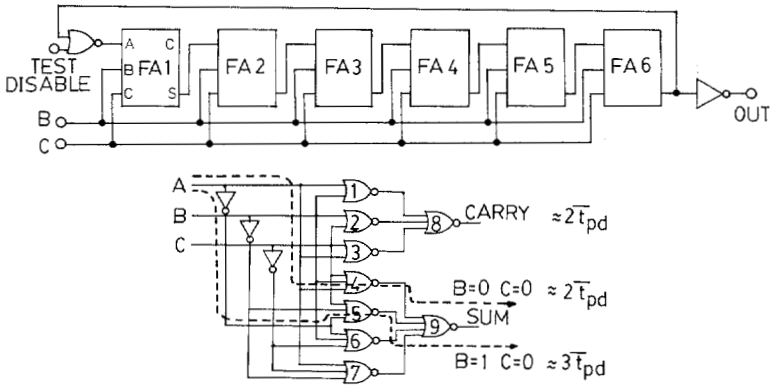

FIGURE 5—Schematic logic diagram of a full adder ring oscillator and a full adder logic circuit. Dashed lines represent the signal propagation path for "B = 0, C = 0" and "B = 1, C = 0" modes. tpd means the average delay time.