Title	A 64K GaAs Gate Array
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[See page 371 for Figure 2.]

SESSION XII: SEMI-CUSTOM ARRAY DESIGN

Chairman: *Tai Sato*
Toshiba Semiconductor
Kawasaki, Japan

THAM 12.1: A 64K GaAs Gate Array*

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TO REALIZE LSI LEVEL INTEGRATION in GaAs, both power dissipation and layout compactness must be carefully considered. From this viewpoint, direct-coupled FET logic (DCFL) has been widely accepted and thought to be the most promising for LSI fabrication[1,2]. However, nothing has been claimed as to its manufacturability, which is doubtful due to the small noise margin problem of DCFL. On the other hand, Buffered FET Logic (BFL), Schottky Diode FET Logic (SDFL) and Source Coupled FET Logic (SCFL) have large immunity to FET threshold voltage deviation. But they consume too much power to be applied to LSIs. This paper will describe a 6K-gate GaAs gate array with a large noise margin and moderate power dissipation circuit, which has been identified as Schottky-diode level-shifter capacitor-coupled FET logic (SLCF)[3]. In addition, a 16b serial-parallel-serial (S/P/S) data conversion circuit, fabricated on this chip, will be covered.

An example of the SLCF circuit is illustrated in Figure 1. There is a level shifting Schottky diode in front of the driver FET, which also acts as a feed-forward capacitor, resulting in rapid switching operation. This circuit offers a larger noise margin than DCFL without sacrificing speed performance and has moderate power dissipation.

This circuit has been applied to a 6K-gate GaAs gate array design and fabrication. Figure 2 shows a photomicrograph of the fabricated chip, in which 232 row x 26 column (= 6032) basic logic cells, 184 I/O buffer cells and 204 pads are included. Chip size is 8.0mm x 8.0mm. Figure 3 shows the layout and equivalent circuit for a basic cell, which measures 128μm x 24μm and can be personalized as either a 2-input NOR or a 2-input NAND gate. The gate width/length are 10/1.0μm, for both driver and load FETs. Between columns, 21 interconnection tracks are provided for 1st-level interconnection with a 2μm design rule for both line and space. Three lines, by 2nd level interconnection with a 3μm design rule, can run across each basic cell. Minimum contact hole size is 2μm x 2μm. An I/O cell is able to be personalized either as an input or an output buffer for Si-ECL interface.

The gate array was fabricated with WN gate self-aligned MESFET process technology[4]. To suppress short-channel effects, lightly-doped drain (LDD) structured FETs were employed. The active layers of FETs and diodes were formed by selective Si ion implantation, with subsequent capless annealing at 850°C for 15 min.. The WN gate metal was deposited by reactive RF magnetron sputtering in Ar + N2 mixed gas. Threshold voltages were set at −0.70V for load FETs and −0.45V for driver FETs. The K-values were measured as to be around 1.3mS/V^2 (Wg = 10μm).

The noise margin for a simple SLCF inverter was measured to be 0.3V, which is large enough to ease constraints as to FET threshold voltage deviation. Propagation delay time (tpd) dependence on interconnection length (L), and the number of fan-ins (FI) and fan-outs (FO) was evaluated by measuring ring oscillators with various loads at V_{DD} = 1.5V and V_{SS} = −1.0V. The unloaded gate delay time was 76ps/gate, and the delay time increased at a rate of 45ps/mm, 10ps/FI and 45ps/FO at 1.2mW/gate power dissipation. This leads to a tpd = 256ps/gate under L = 2mm and FO = 3 loading condition. The features of the gate array are summarized in Table 1.

A 16b serial-parallel-serial (S/P/S) data conversion circuit was constructed as an application example of this gate array. Figure 4 shows a logic diagram for an S/P/S data conversion circuit. It consists of a 16b input shift register, a 16b parallel latch, a 16b output shift register with multiplexers, a counter circuit and a clock driver. This circuit is constructed with 38 edge-trigger flip-flops, 16 latches, 15 two-input multiplexers, 110 NOR gates and 22 I/O buffers. The clock distribution scheme was designed for maximum operating speed: 579 basic cells were used, and occupied approximately 20% of the area of the gate array. High-speed testing was performed directly on a wafer using a 50Ω measurement system. Typically, the circuit operated at clock rate of 700Mb/s. The maximum data rate found among the measured chips was 852Mb/s. The input and output waveforms for 754Mb/s operation are shown in Figure 5, where the power dissipation was 689mW for the S/P/S data conversion function and 186mW for the I/O buffers with V_{DD} = 2.0V and V_{SS} = −1.0V. This speed means that the gate delay time for the critical path inside the circuit was 220ps/gate, which agrees approximately, with the measurement data on ring oscillators.

Acknowledgments

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[2] Toyoda, N., et. al., "A 2K-gate GaAs Gate Array with a WN Gate Self-Aligned FET Process", *IEEE J. Solid-State Circuits*, Vol. SC-20, p. 1043; Oct., 1985.

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[4] Uchitomi, N., et. al., "Refractory WN Gate Self-Aligned GaAs MESFET Technology and its Application to Gate Array ICs", *Extended Abstracts of the 16th Conference on Solid-State Devices and Materials*, p. 383; 1984.

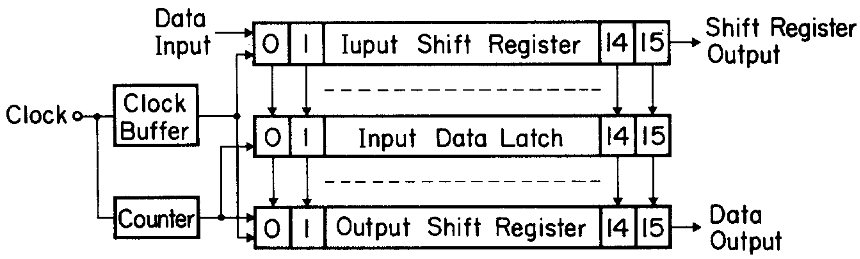

FIGURE 4—Logic diagram of a 16b serial-parallel-serial data conversion circuit.

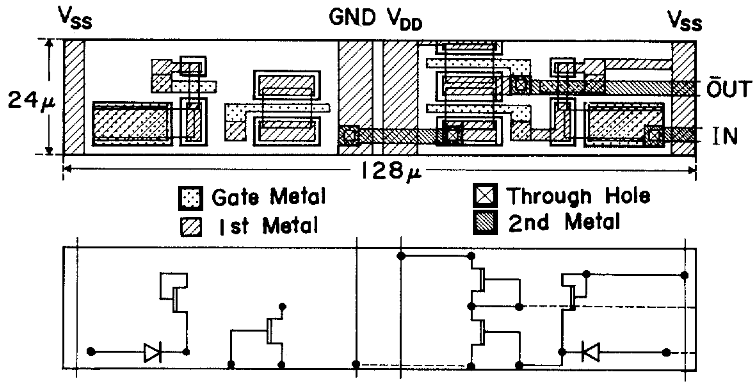

FIGURE 3—Basic cell layout and equivalent circuit.

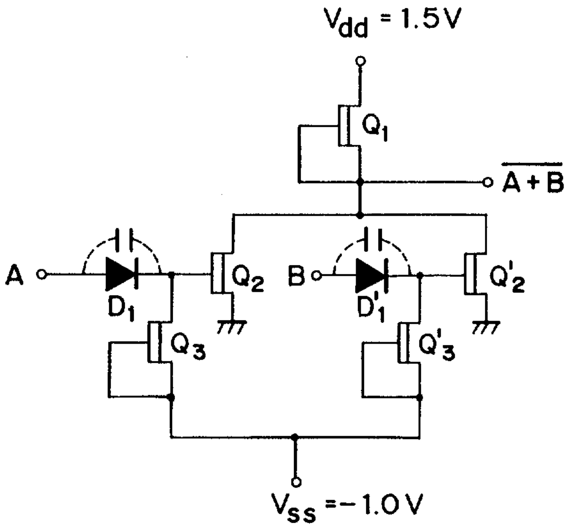

FIGURE 1—Input NOR gate implemented by SLCF circuitry.

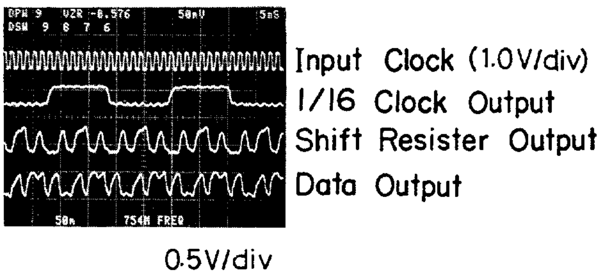

FIGURE 5—Waveforms for a 16b S/P/S data conversion circuit at 754Mb/s data rate.

Chip size	8.0mm x 8.0mm
Circuitry	SLCF
Basic cell size	128μm x 24μm
Number of basic cells	6032 (232 row x 26 column)
Number of I/O	184 (max.)
Number of pads	204 (including I/O)
Power Supply	+1.5V, –1.0V
Device size	10μm/1.0μm load and driver FETs
	2μm/2.0μm pull-down FET
	6μm x 10μm Schottky diode
Design rule for interconnection	
1st level	2μm (width and space)
2nd level	3μm (width and space)
Through hole	2μm x 2μm
FET performance (measured)	
Vth	–0.45V (driver FET)
	–0.70V (load FET)
K-value	$1.3mA/V^2$ (Wg = 10μm)
Propagation delay time	
Unloaded (Fan-out = 1)	76ps/gate
Dependence on load	10ps/Fan-in
	45ps/Fan-out
	45ps/mm
Power dissipation	1.2mW/gate

TABLE 1—Features of 6K-gate GaAs gate array.

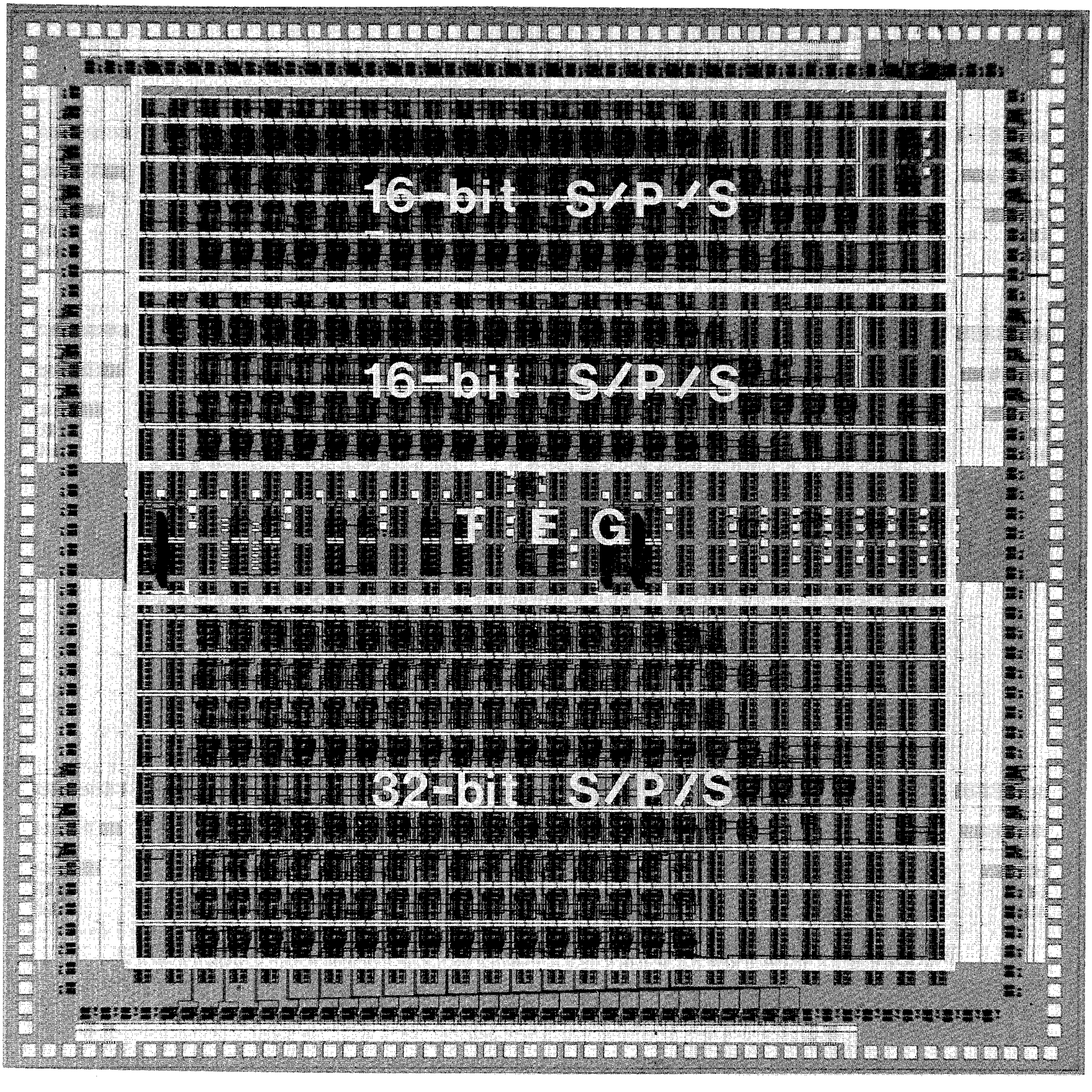

FIGURE 2–Microphotograph of 6K-gate GaAs gate array, on which ring oscillators with various loads and S/P/S data conversion circuits were constructed.