A 2K-Gate GaAs Gate Array with a WN Gate Self-Alignment FET Process

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Abstract—**A 2K-gate DCFL GaAs gate array has been successfully fabricated with a WN gate self-alignment GaAs MESFET process. Chip size was 4.59 mm×4.73 mm. A basic cell, consisting of one DFET and three EFET's, can be programmed as an inverter, or a two or three-INPUT NOR gate by personalizing with first- and second-level interconnection and via hole masks. The I/O buffer was implemented with a large DCFL push–pull circuit.**

The unloaded propagation delay time was 42 ps/gate at a power dissipation of 0.5 mW/gate. The increase in delay time due to various loading capacitances were 11-ps/fan-in, 16-ps/fan-out, 59-ps/1-mm interconnection and 0.95 ps/crossover (area: 2 μm×3 μm).

An 8×8-bit parallel multiplier was fabricated on this gate-array chip. A multiplication time of 8.5 ns was achieved at a power dissipation of about 400 mW including I/O buffers.

I. INTRODUCTION

IN ORDER to increase the speed of microelectronic systems, it is advantageous to reduce the interchip signal delay by maximizing the device integration level. As the integration level increases, however, the development time becomes longer. Quick development of new LSI is increasingly important because the product life cycle has been becoming shorter. A gate-array approach is effective under these circumstances. Very high-speed IC such as Si bipolar ECL logic is no exception, and 2.5–9.0K-gate gate arrays with 0.30–0.50-ns loaded gate delay have been developed [1]–[4]. However, very large power consumption, 5–20 W/chip, limit their field of applications. Gallium arsenide gate arrays have attracted much interest as a replacement for Si ECL gate arrays because of smaller gate delay and lower power consumption. To date, 300–1K-gate GaAs gate arrays have been reported [5]–[8]. Their loaded delay times were about 300–600 ps/gate. These performances cannot fully encourage the system designer to select GaAs gate arrays because they require higher speed and higher integration. Under such circumstances, we determined that the target of this work is a 2K-gate gate array with a loaded delay time less than 300 ps/gate as a first step to develop high-speed and high-integration GaAs gate arrays.

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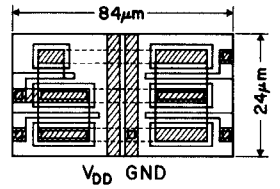
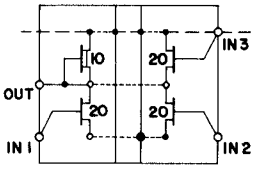


(a)



(b)

Fig. 1. (a) Pattern layout and (b) equivalent circuit of a basic cell. Each number means the gate width in micrometers.

This paper describes the design of the master chip, the fabrication process, the performance of a basic gate, and an application to an 8×8-bit parallel multiplier.

II. MASTER CHIP DESIGN

A. Basic Cell

Fig. 1 shows (a) the pattern layout and (b) the equivalent circuit of a basic cell. It consists of one DFET ($W/L = 10/1.5$) and three EFET ($W/L = 20/1.5$), where W and L mean the gate width and length on the mask in micrometers. Power supply (V_{DD}) and ground (GND) lines, which are made with a 5-μm-wide first interconnection metallization, run at the center of each cell. The dimension of one basic cell is 84 μm×24 μm. One basic cell can be programmed as an inverter, or a two- or three-input NOR gate by personalizing with three masks, i.e., first/second interconnections and via hole.

The target values of the threshold voltage for the E- and DFET's were determined by using SPICE simulation. Fig. 2 is the simulated noise margin and the expected propagation delay time in an inverter as a function of the threshold voltages of the EFET (V_{TE}) and DFET (V_{TD}). The main SPICE parameters were $K = 1.35$ mA/V^2 ($W =$

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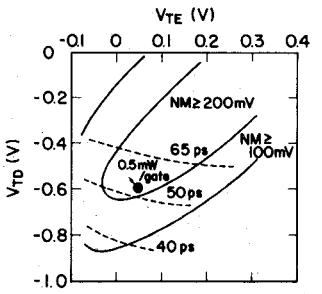

Fig. 2. Noise margin (NM) and propagation delay time as a function of the threshold voltage of EFET (V_{TE}) and DFET (V_{TD}). Closed circle is the target.

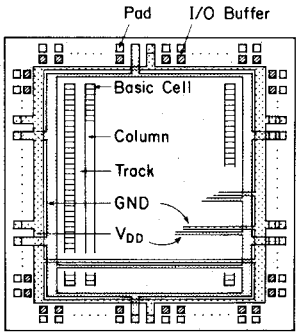

Fig. 3. Schematic drawing of a 2K-gate GaAs gate array chip. Chip size is 4.59 mm×4.73 mm.

10 μm), $\lambda = 0.1$ (1/V) for EFET, and $K = 1.20$ mA/V^2 ($W = 10$ μm), $\lambda = 0.1$ (1/V) for DFET, which were empirically obtained for a 1.0–1.2-μm gate self-aligned GaAs MESFET.

B. Cell Layout

Fig. 3 shows the schematic drawing of a 2K-gate gate array chip, in which 112 row×18 column (= 2016) basic cells, 66 I/O buffer cells, and 68 pads are included. Chip size is 4.59 mm×4.73 mm. Between columns, 15 interconnection tracks were prepared for 2-μm-wide first-level interconnection lines with 3-μm spacings. Three second-level interconnection lines with the design rule of 3-μm width and 4-μm spacing can run over each basic cell. The minimum size of a contact hole is 2 μm×2 μm. Input and output (I/O) buffers are implemented with large (W/L = 200/1.5 for EFET and W/L = 100/1.5 for DFET) DCFL push–pull circuits.

The noise margin in a DCFL circuitry is approximately 200 mV at best as shown in Fig. 2. Thus V_{DD} voltage drop and GND voltage rise must be suppressed as much as possible together with the precise control of the threshold voltage of FET's. This is an annoying problem in the design of GaAs DCFL IC's, especially when the gate count increases. In this work, the V_{DD} and GND line width and their distribution were carefully designed. Fig. 4 is the pattern of GND line in a 2K-gate gate array chip. A main GND line surrounds the basic cell arrays. The left and right main lines are 150 μm in width with two pads because the current mostly flows to left and right sides, while top and bottom main lines are narrow, 40 μm, with

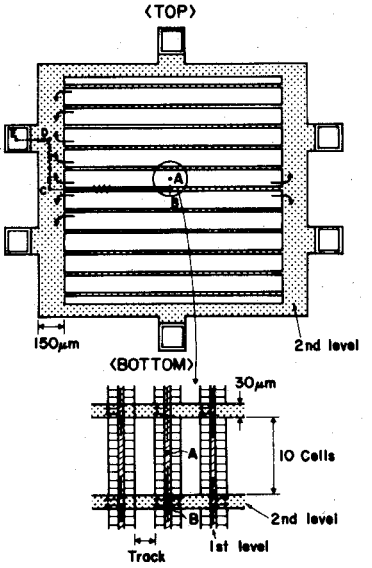

Fig. 4. Ground line pattern in a 2K-gate gate array chip.

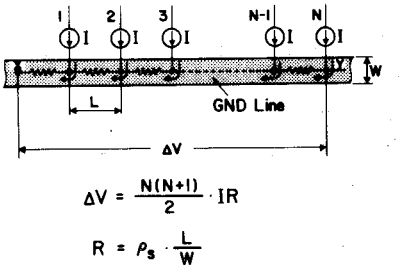

Fig. 5. Potential difference along GND line due to periodic current inflow.

one pad. Subsidiary GND lines are horizontally distributed every ten basic cells. Their width is 30 μm. Both the main and subsidiary GND lines are fabricated in the second-level interconnect metallization (sheet resistivity = 0.03 $\Omega/\square$) because of lower resistivity than that of first-level metallization (sheet resistivity = 0.15 $\Omega/\square$). If all the basic cells are used, the potential at point A in the vicinity of the chip center becomes highest. When the current I, flows into a ground line with a constant pitch L, as shown in Fig. 5, the potential difference V_{x-y} between X and Y points is $N(N+1)\cdot IR/2$. Using this formula, the potential difference between point-A and point-B, point-B and point-C, point-C and point-D, and point-D and point-E can be calculated as 5, 30, 11, and 6 mV, respectively. That means the GND potential becomes about 50 mV at worst. The amount of V_{DD} voltage drop in the worst case is also calculated at about 130 mV. These values are insufficient to assure the stable operation in DCFL. However, we decided to adopt this V_{DD} and GND line architecture because the utilization ratio of the basic cell array is supposed to be 60–70 percent in the fabrication of actual devices on this gate array.

III. Fabrication

A self-alignment GaAs MESFET process is indispensable in order to realize high-performance GaAs DCFL IC's. Among several process technologies, a refractory metal

or metallic compound gate self-aligned FET process, being similar to poly-Si gate Si MOSFET widely used in Si MOS LSI's, is the most promising. The key point in this technology is the selection of refractory gate material. Titanium–tungsten (TiW) or tungsten–silicide (WSi_x) has been used. Recently, we have found that tungsten–nitride (WN_x) is superior to other refractory metal or metallic compounds because of lower film resistivity ($\rho \approx 70\ \mu\Omega \cdot$cm) and larger Schottky barrier height ($\phi_B \approx 0.80 \sim 0.85$ V) to n-type GaAs active layer [14]. These features are very attractive for GaAs DCFL IC's.

The fabrication process is as follows. Active channel layers for E- and DFET's were formed by $^{28}Si^+$ selective implantation into undoped semi-insulating 2-in-diam GaAs LEC wafers at 50 keV with doses of 1.9×10^{12} cm^{-2} and 3.5×10^{12} cm^{-2}. Post implantation annealing was performed at 850°C for 15 min in $Ar+AsH_3$ without any encapsulating films. The tungsten–nitride film was deposited by reactive RF sputtering in $Ar+N_2$ (6-percent) mixed gas. After photolithographic delineation for the gate electrode pattern, the WN_x film was etched by RIE with CF_4+O_2 gas. In this pattern transfer process, the gate length becomes about 0.4–0.5-μm smaller than that on the mask. In other words, the actual gate metal length was about 1.0–1.1 μm. Source and drain region were formed by $^{28}Si^+$ implantation at 180 keV with a dose of 3×10^{13} cm^{-2} and successive PSG cap annealing at 800°C for 10 min. The ohmic contact was AuGe/Au. The first- and second-level interconnection metallizations were Ti/Pt/Au. The Au film thickness differs between first and second levels, resulting in the sheet resistivities of $\rho_s = 0.150\ \Omega/\square$ for first and $\rho_s = 0.03\ \Omega/\square$ for second levels as mentioned above. The interlayer insulating film was SiO_2 of 6000-Å thickness.

IV. Basic Gate Performance

In order to evaluate the performance of the gate array, several test circuits (five types of 15-stage ring oscillators, a six-stage full adder ring oscillator and an 8×8 bit parallel multiplier) were fabricated on the same master chip as shown in Fig. 6.

Fig. 7 shows the propagation delay time (t_{pd}) as a function of power dissipation (P_d) under various loading conditions. All of the raw data obtained from three different wafers (#25, #40, #67) are plotted. The threshold voltage (V_{TD}) variation of DFET in a wafer and among wafers leads to the wide distribution of t_{pd} and P_d. As shown in Fig. 2, the designed value of DFET threshold voltage is −0.60 V which approximately corresponds to the power dissipation of 0.5 mW/gate. Table I thus summarizes the propagation delay times at $P_d = 0.5$ mW/gate, which are picked up from Fig. 7. The loaded propagation delay time is empirically given by

$$t_{pd} = t_{pd0} + (I-1)\Delta t_{pd/\mathrm{FI}} + (F-1)\Delta t_{pd/\mathrm{FO}} + L\Delta t_{pd/\mathrm{LINE}} + N\Delta t_{pd/\mathrm{CO}}, \quad (1)$$

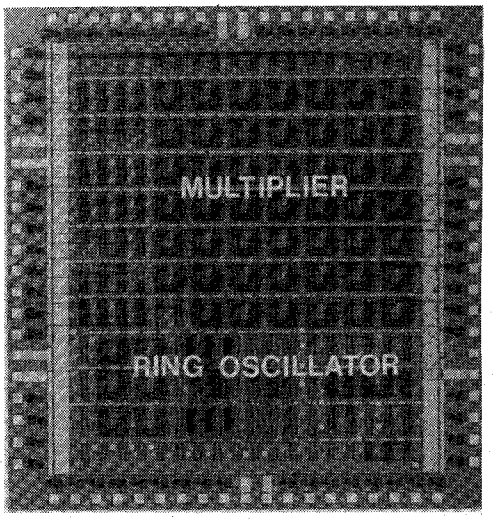

Fig. 6. Photomicrograph of a 2K-gate GaAs gate array on which five types of ring oscillators, a full-adder ring oscillator and an 8×8-bit parallel multiplier were fabricated.

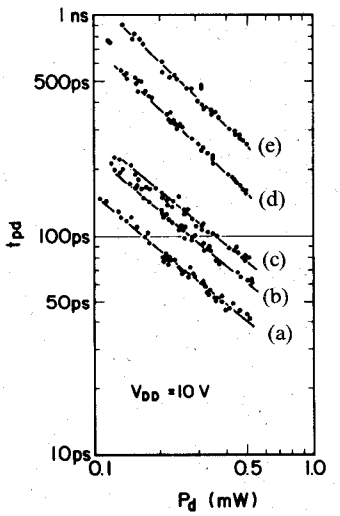

Fig. 7. Propagation delay time (t_{pd}) as a function of power dissipation (P_d) under various conditions. (a) FI = 1, FO = 1, (b) FI = 3, FO = 1. (c) FI = 1, FO = 3. (d) FI = 1, FO = 1, 2-mm interconnection. (e) FI = 1, FO = 1, 2-mm-interconnection, 100 crossovers (area: 2 μm×3 μm).

TABLE I
Propagation Delay Times Under Various Loading Conditions

Loading Conditions			tpd
F.I.=1	F.O.=1		42 ps
F.I.=3	F.O.=1		63 ps
F.I.=1	F.O.=3		75 ps
F.I.=1	F.O.=1	L=2mm	160 ps
F.I.=1	F.O.=1	L=2mm	255 ps
C.O.=100			

P_d =0.5 mW/gate

Note: "C0-100" means that the 2-mm-long first-level interconnection line crosses over the grounded second-level interconnection line 100 times between each inverter.

where

t_{pd0} unloaded (FI = FO = 1) propagation delay time,

$\Delta t_{pd/\mathrm{FI}}$ increase in delay time per fan-in,

TABLE II
DELAY TIME INCREMENTS DUE TO FAN-IN, FAN-OUT, INTERCONNECTION LINE, AND CROSSOVER CAPACITANCES

Δt_{pd}/FI	11	ps/FI
Δt_{pd}/FO	16	ps/FO
Δt_{pd}/LINE	59	ps/mm
Δt_{pd}/C.O.($2\times3\mu^2$)	0.95	ps/C.O.

P_d = 0.5 mW/gate

TABLE III
COMPARISON OF BASIC GATE PERFORMANCES AMONG RECENT HIGH-SPEED GATE ARRAYS

	CMOS/SOS[9]	ECL(1)[3]	ECL(2)[4]	THIS WORK
Gate Count	8K	2.5K	9K	2K
Gate Delay*1 (t_{pd})	0.67ns	0.27ns	0.30ns	0.215ns
Power Dissipation*2	0.05mW*3	2.6mW	6mW	0.5mW
Gate length or Emitter width *4	1.8μm	0.5μm	—	1.1μm

*1 FI = 3, FO = 3, 2mm-interconnection
*2 power dissipation per gate
*3 operation frequency = 12.5 MHz
*4 actual length or width

$\Delta t_{pd/FO}$ increase in delay time per fan-out,
$\Delta t_{pd/LINE}$ increase in delay time per unit interconnection line length,
$\Delta t_{pd/CO}$ increase in delay time per one crossover,
I, F, N number of fan-in, fan-out and crossover, and
L interconnection line length.

Using data shown in Table I and this equation, the increase in delay time due to fan-in, fan-out, interconnection line, and crossover capacitances were calculated and are shown in Table II. The loaded propagation delay time is important rather than unloaded delay time when we fabricate actual IC's using a gate array. If the average loading condition is postulated to be fan-in = 3, fan-out = 3, interconnection line length = 2 mm, which is similar loading condition usual for Si ECL or CMOS gate array, the loaded delay time becomes 215 ps.

Recently, advanced Si CMOS and Si ECL gate arrays have been reported. Their performances are compared with this work in Table III. It is found that a 2K-gate GaAs array is the fastest with a medium power dissipation.

V. AN 8×8-BIT PARALLEL MULTIPLIER

Fig. 8 shows the schematic logic diagram of an 8×8-bit parallel multiplier circuit employing a carry save scheme. It consists of 8 half adders (HA), 48 full adders (FA), 64 NOR gates (NOR), and 32 I/O buffers. 728 basic cells were used and approximately 50 percent of gate-array area was occupied.

The maximum multiplication time (T_{MUL}) is obtained when the partial product A_7B_0, propagates through the critical path to P_{14} as shown in Fig. 8. Therefore, high-speed testing was performed on the wafer, which had passed the

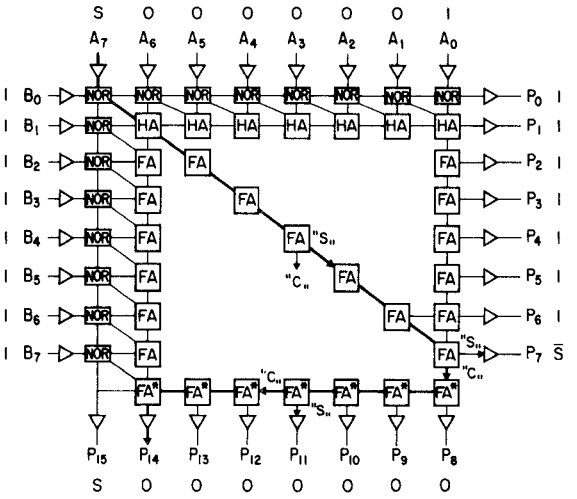

Fig. 8. Logic diagram of an 8×8-bit parallel multiplier. NOR: NOR gate, FA: full adder with NOR gate, FA*: full adder, HA: half adder with NOR gate, HA*: half adder. "S" is SUM signal and "C" is CARRY signal.

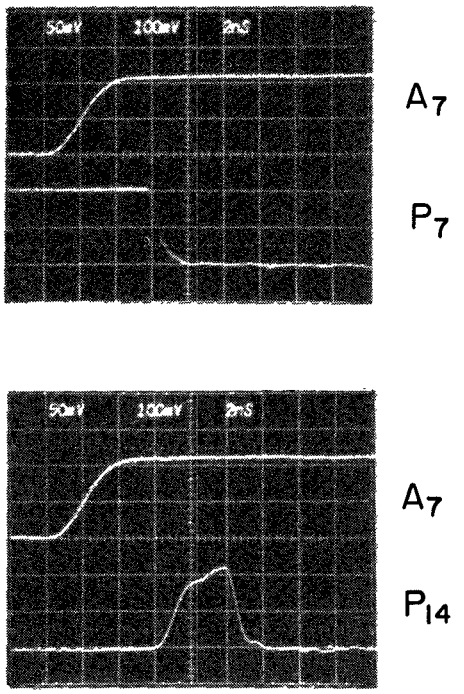

Fig. 9. Input pulse (S) applied to A_7 and output waveforms at P_7 and P_{14} when $A(=$ S0000001$)\times B(11111111)$ multiplication was performed.

low-frequency functional testing, with input codes of $A =$ S0000001 and $B = 11111111$. Here S means the pulse input. Fig. 9 shows an example of the input pulse applied to A_7 and the output waveforms which appeared at the P_7 and P_{14} output pads. The delay times were 4.4 and 8.5 ns, where the power dissipation was 228 mW for an 8×8-bit parallel multiplier block and 176 mW for 32 I/O buffers.

If the CARRY and SUM signal delay time in a full adder is known, the multiplication time (T_{mul}) can be predicted by using the following:

$$T_{mul} = t_{NOR} + \left(t_c^{HA} + t_s^{HA}\right) + 6\left(t_c^{FA} + t_s^{FA}\right) + 2t_{BUF} + 7\left(t_c^{FA} + t_s^{FA}\right) \quad (2),$$

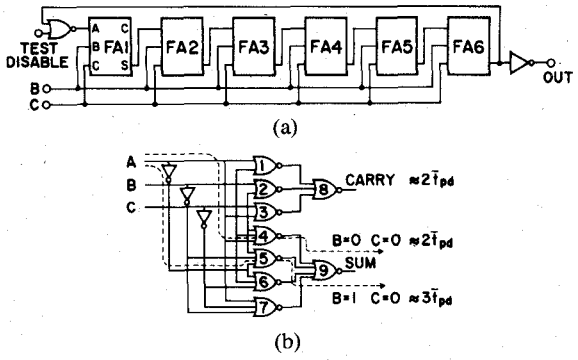

Fig. 10. Schematic logic diagram of (a) a full-adder ring oscillator and (b) a full-adder logic circuit. Dashed lines represent the signal propagation path for "$B=0$, $C=0$" and "$B=1$, $C=0$"-modes. t_{pd} means the average delay time.

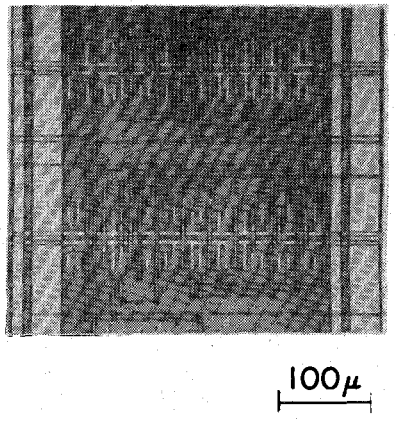

Fig. 11. Photomicrograph of a full adder after personalizing.

where t_{NOR}: NOR gate delay time t_s^{HA}, t_c^{FA}: sum and carry delay times in a half adder, t_{BUF}: I/O buffer circuit delay time. The CARRY and SUM signal delay times are obtained from a full-adder ring oscillator. Fig. 10 is the schematic logic diagram of (a) a six-stage full-adder ring oscillator and (b) a full adder. There are two ring oscillation modes. From the $B=0$, $C=0$-mode ring oscillation, the propagation delay time when the signal passes through two NOR gates (no. 4 and no. 9) is experimentally obtained. The CARRY signal propagation delay time, t_c^{FA}, is almost equivalent to this time. The SUM signal propagation delay time t_s^{FA}, is directly obtained from the $B=1$, $C=0$-mode ring oscillation.

The measured values were $t_c^{FA}=540$ ps and $t_s^{FA}=670$ ps which were obtained in the same chip (no. 25-3-2) where the performance of a multiplier shown in Fig. 9 was measured. Putting $t_c^{FA}=540$ ps and $t_s^{FA}=670$ ps into (2), the multiplication time becomes 8.47 ns which agrees well with the directly measured value (8.5 ns) shown in Fig. 9.

There still remains a question whether the performance of a full-adder circuit can be consistently explained by using the basic data provided from a ring oscillator. We discuss this problem below.

The delay times in a full adder for "$B=0$, $C=0$" and "$B=1$, $C=0$"-modes are calculated from the following:

$$t_c^{FA} \quad t_{pd}(\mathrm{FI}=3, \mathrm{FO}=1, L=L_1, N=N_1) + t_{pd}(\mathrm{FI}=4, \mathrm{FO}=5, L=L_2, N=N_2) \quad (3)$$

$$t_s^{FA} \quad t_{pd}(\mathrm{FI}=1, \mathrm{FO}=2, L=L_3, N=N_3)+t_c^{FA}. \quad (4)$$

In an actual full-adder circuit (Fig. 11) on the 2K-gate gate array L_1, L_2 and L_3 were approximately 0.25, 1.25, and 0.30 mm, and the effective number of crossovers N_1, N_2, and N_3 were 4, 26, and 4, respectively.

In the no. 25-3-2 chip for which a multiplier and a full-adder ring-oscillator performance were measured, the propagation delay times obtained from the ring oscillator were 70 ps (FI = FO = 1), 106 ps (FI = 3, FO = 1), 130 ps (FI = 1, FO = 3), 296 ps (FI = FO = 1, $L=2$ mm) and 480 ps (FI = FO = 1, $L=2$ mm, CO = 100) at a power dissipation of 0.26 mW/gate, resulting in $\Delta t_{pd/\mathrm{FI}}=18$ ps/FI, $\Delta t_{pd/\mathrm{FO}}=30$ ps/FO, $\Delta t_{pd/\mathrm{LINE}}=113$ ps/mm and $\Delta t_{pd/\mathrm{CO}}=1.8$ ps/crossover. Putting these values into (3) and (4), t_c^{FA} and t_s^{FA} become 573 ps and 713 ps which agree fairly well with the experimental values of $t_c^{FA}=540$ ps and $t_s^{FA}=670$ ps. This result indicates that the performance of actual circuits fabricated on this gate array can be well predicted from the basic switching performances obtained from simple ring oscillators.

TABLE IV
COMPARISON OF MULTIPLIER PERFORMANCES IN AN 8×8-BIT PARALLEL MULTIPLIER

CMOS/SOS* [10]	Gate Array	~12.5 ns	~ 40 mW
ECL [11]	Custom	10.0 ns	660 mW
ECL [2]* [3]	Macrocell Array	~ 3.5 ns	~500 mW
GaAs [1] [12]	Custom	5.25 ns	610 mW
GaAs [2]* [13]	Custom	~ 5.3 ns	~238 mW
THIS WORK measured	Gate Array	8.5 ns	400 mW
estimated		~ 5.0 ns	~600 mW

* The data in a N×N bit multiplier is converted to an 8×8 bit multiplier by the following equations.

$$\begin{bmatrix} T_{MUL} \approx (N-1)(t_s^{FA}+t_c^{FA}) & T_{MUL}(8\times8)/T_{MUL}(N\times N)=7/(N-1) \\ P_d \approx N(N-1)\cdot P_d^{FA} & P_d(8\times8)/P_d(N\times N)=56/N(N-1) \end{bmatrix}$$

The multiplier did not completely operate in the chips where the threshold voltage of DFET is at around −0.60 V (designed value) and the propagation delay times under various loading conditions are similar to the values shown in Table I. Thus, we cannot actually demonstrate here the potential of this gate array with the multiplier performance. However, it can be estimated by (2), (3), and (4) with the data in Table II. The calculated result is $T_{MUL} \approx 5$ ns.

Finally, in Table IV we compare the 8×8-bit parallel multiplier performance in this study with those previously reported.

VI. SUMMARY

A 2K-gate GaAs DCFL gate array was fabricated. A basic cell architecture allows the implementation of an inverter, or a two- or three-input NOR logic function by personalizing with three masks, i.e., first- and second-level

interconnection and via hole. Ground (GND) and power supply (V_{DD}) line distribution within a chip was carefully designed in order that the GND and V_{DD} voltage drop or rise would not exceed 50 mV. This gate array was fabricated with a tungsten–nitride (WN_x) gate GaAs MESFET process similar to poly-Si gate Si MOSFET process, which promises the large driving capability in a normally-off GaAs MESFET. Several test circuits were fabricated to investigate the performances of this gate array. Five types of 15-stage ring oscillators revealed that unloaded delay time was 42 ps/gate at a power dissipation of 0.5 mW, and the increase of delay time due to various loading capacitances were 11 ps/FI, 16 ps/FO, 59-ps/1-mm interconnection and 0.95 ps/crossover, resulting in the loaded propagation delay time of 215 ps under the conditions of FI = 3, FO = 3, and 2-mm interconnection. This value is the smallest among advanced high-speed Si CMOS/SOS, Si bipolar ECL and other GaAs gate arrays. An 8×8-bit parallel multiplier was also fabricated on this gate array. A multiplication time of 8.5 ns was achieved when the power dissipation was 400 mW, including I/O buffer circuit.

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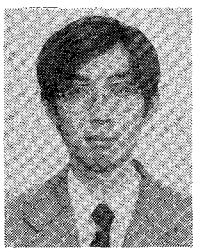

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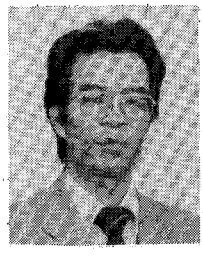

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