A One-Day Chip: An Innovative IC Construction Approach Using Electrically Reconfigurable Logic VLSI with On-Chip Programmable Interconnections

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Abstract—**A new custom IC design methodology and the associated logic VLSI chip, which offer an ultimately fast turnaround-time logic IC construction method, are proposed.**

Using the new VLSI chip, digital system and logic designers can construct their own real IC chip with thousands of logic gates, as easily as if they drew logic diagrams to be implemented in the form of a printed-circuit board, which would utilize standard logic IC families. This construction can even be carried out in a second, because logic structures can be reconfigured electrically, due to on-chip programmable interconnection capability. This chip contains various kinds of logic functional blocks, such as inverters, NOR's, NAND's, flip-flops, shift registers, counters, adders, multiplexers, ALU's, and so on. Up to 200 SSI/MSI standard logic blocks can be provided. The E^2PROM-type MOSFET switch matrix is adjacent to the functional blocks, in order to connect any output to specific inputs of the functional blocks. It also offers a ready-to-test aid, obtained by monitoring the signal waveform developed inside the chip.

These features have the advantage over the present custom IC design methods, such as gate array, standard cell, silicon compiler, or programmable logic array (PLA) approaches, in the sense that the designer can easily redesign the logic to obtain a digital system in an IC even within one day.

I. INTRODUCTION

GREAT PROGRESS in semiconductor devices has been made since the invention of the transistor in 1947. Highlights, which made major breakthroughs toward higher integration of electronic components, include integrated circuits and microprocessors. The advanced IC fabrication technology now enables hundreds of thousands of logic gates to be integrated in a chip. This technology has been successfully applied to memory IC's of megabits per chip level. However, the logic IC's do not fully enjoy this technological potential. There is a diversely wide range of logic systems which are desired to be implemented in the form of IC's. However, only mass-produced circuits, such as general purpose microprocessors, can be cost effective in the category of custom logic IC's. This is because the development time ranges from a month to a year, which makes frequent redesign of a logic expensive and impractical.

Gate array, standard cell, and silicon compilation are methodologies applied to ease this constraint [1]. However, they still require physical and chemical processing time which is too long for system and logic designers to effectively redesign their ideas. Faster turnaround time is still strongly desired. On the contrary, programmable logic array (PLA) type circuits are available with field programming capability [2], [3]. The logic can be created in a relatively short period of time. This style is restrictive, because programming is basically carried out in terms of Boolean algebra, which cannot be applied to sequential logical circuits. Recently, there have been improved PLA versions [3], which have feedback loops, but they are not advanced enough to let designers feel they are friendly, because most of system ideas are not created in the designer's brain in the form of Boolean algebra. As a result, a large number of small volume logics still remain in the form of a printed-circuit board, instead of being implemented in custom IC's.

It is therefore the purpose of this paper to present a VLSI chip that provides system and logic designers with an innovative IC construction method.

II. CONCEPT OF THE NEW DESIGN METHOD

Using the proposed VLSI, a designer can construct an actual IC chip with more than several thousand logic gates, as if they drew logic diagrams to be implemented in the form of a printed-circuit board, which would utilize standard logic IC families. This construction is carried out in even a few seconds, because logic structure can be reconfigured by changing the interconnections electrically. In addition, it offers frequent reconstruction capability.

Fig. 1 shows a conceptual drawing of this VLSI. Fifty to 200 standard logics of SSI/MSI level integration act as functional blocks and are placed in a chip that is ap-

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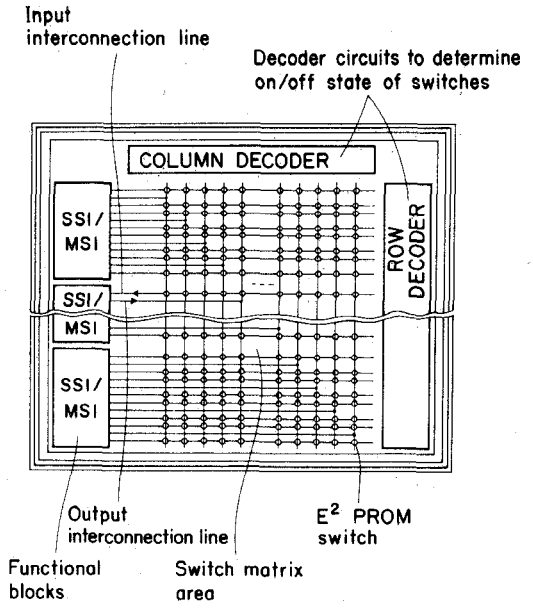

Fig. 1. Conceptual drawing of the proposed VLSI.

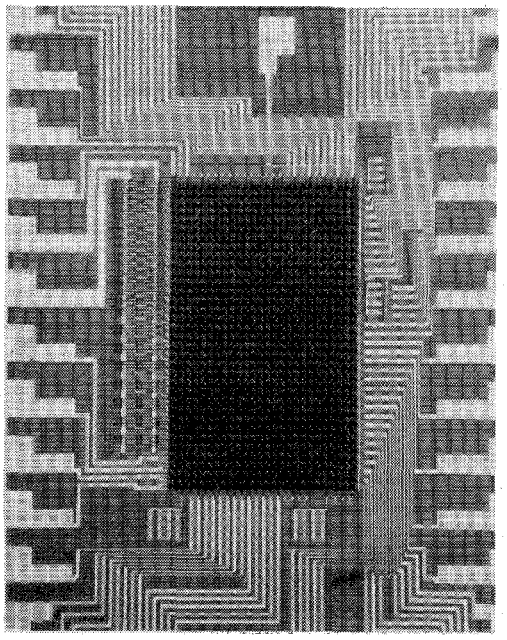

Fig. 2. Photomicrograph of the fabricated test chip. The switch matrix has 34-row × 26-column switches and occupies an 850 × 520-μm area.

proximately 10 × 10 mm in size. Inputs and outputs from functional blocks are introduced into the switch matrix area to be connected to any of the desired I/O terminals by selecting the switch that should be turned on. Each switch is realized by E²PROM-type floating gate MOSFET. The ON/OFF state is kept unchanged, once the state is written. ON switch selection might correspond to the interconnection layout in the conventional custom IC design work, or to the wire lapping work in IC board construction. It is therefore very important to make propagation delay times comparable to those in the printed-circuit board, which is in the range of 1 ns to 20–30 ns. To do this, an output buffer circuit is introduced at each output of the functional block.

The designer can easily change the wiring by designating the switches to be turned on and off, which is accomplished in a drastically short period of time (around a second) and at low cost, compared with the conventional circuit board or custom IC fabrication approach. In addition, this new method offers a logic testing aid. By extending one of the matrix lines to outside the chip and designating a specific switch along the line, the designer can monitor the logic state or even the waveform developed at any node inside the circuit. This is very similar to the probing and the checking of the waveform on the oscilloscope, which is usually carried out in the circuit board design. In this sense, the present VLSI chip is completely different from PLA, which basically carries out programming for the logics that can be expressed in terms of Boolean algebra.

III. Test Chip

Fig. 2 shows a photomicrograph of the fabricated test chip. It has 14 inverters, eight two-input NAND gates as functional blocks, and a 34-row × 26-column switch matrix. It also has four I/O terminals for signals in and out of an IC. Any output can be connected to any desired input through the switch matrix.

An individual switch is realized by dual-control cell-type E²PROM floating-gate MOSFET ($W_g/L_g = 5\ \mu m/1.5\ \mu m$) [4], and is placed at each crossing point for the output line and the input line. Three types of switch cells are used, as seen in Fig. 3 which summarizes the test chip configuration. Each switch cell has a 25 × 20 μm size. Individual switch cell types connect or disconnect an output line and an input line that cross each other in the switch cell. Every cell has one input line running horizontally. In the type I switch cell, there is only one output line, which runs vertically. In the type II, horizontally and vertically running output lines form *T*-shapes to physically connect each other. In the type III, there are two kinds of output lines, one of which runs horizontally, that is, electrically independent from other vertically running output lines. The reason why these three kinds of switch cells are required is implied in Fig. 1. Fig. 4 shows a schematic representation of a switch-cell cross section, designed specially for the new VLSI chip. It has a WRITE/ERASE electrode, which performs ON/OFF writing by using tunnel oxide, causing no interference with a signal that passes through the switch. Plus/minus 20-V voltage was applied to the column and row select stacked gates to write the OFF/ON state for the switch, which was accomplished within 1 ms.

For process simplicity, triple-layer polysilicon lines and single-layer Al lines were used. Decoder circuits for the E²PROM switch were intentionally omitted in the first version of the chip, to evaluate the principal operation of the new VLSI.

The ON-state switch allowed 1-mA current flow, as shown in Fig. 5. Signal waveform, which was transmitted through an ON switch, was also measured, when 220-pF capacitive

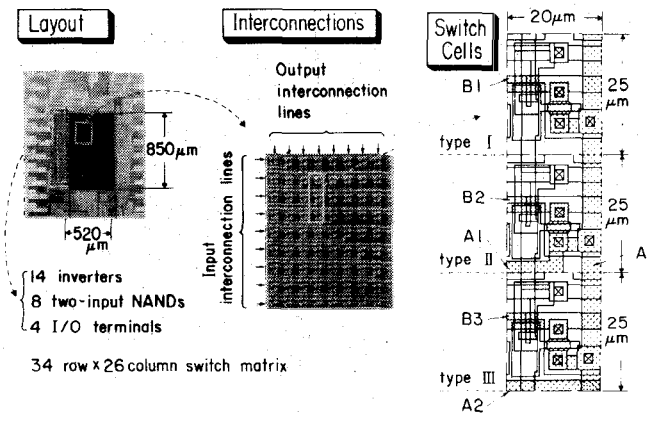

Fig. 3. Configuration of the test chip. The chip has 14 inverters, eight two-input NAND gates as functional blocks, four I/O terminals, and a 34-row×26-column switch matrix. An output interconnection line runs from each functional block into the switch matrix area, forming a *T*-shape to run vertically. An input interconnection line runs horizontally, forming crossing points with output interconnection lines. Also shown are the three types of switch cells. *A*1, *A*2: Output interconnection lines. *B*1, *B*2, *B*3: Input interconnection lines.

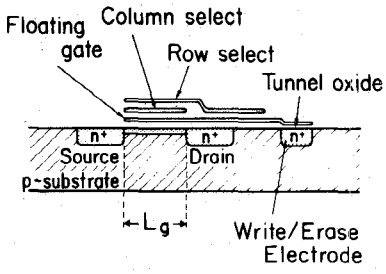

Fig. 4. Schematic representation of a cross-sectional view of an E^2PROM-type switch.

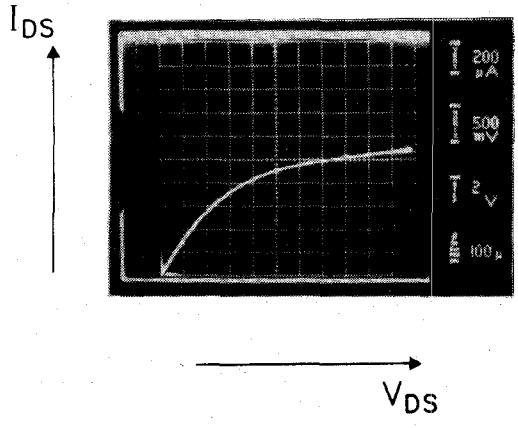

Fig. 5. Measured $I-V$ characteristic for the fabricated E^2PROM-type MOSFET switch under ON state. $W_g/L_g = 5\ \mu m/1.5\ \mu m$.

load existed on the input interconnection line. The result is shown in Fig. 6. The transmission delay is found to be around 2 μs, which means that the signal delay in the switch matrix is about 10-ns/pF parasitic capacitance along the input interconnection line. Signal rise/fall time on the output interconnection line is determined by the current drivability of the output buffer in the functional block and the parasitic capacitance along the output interconnection line. Therefore it is much quicker than the signal transient developed on the input interconnection line.

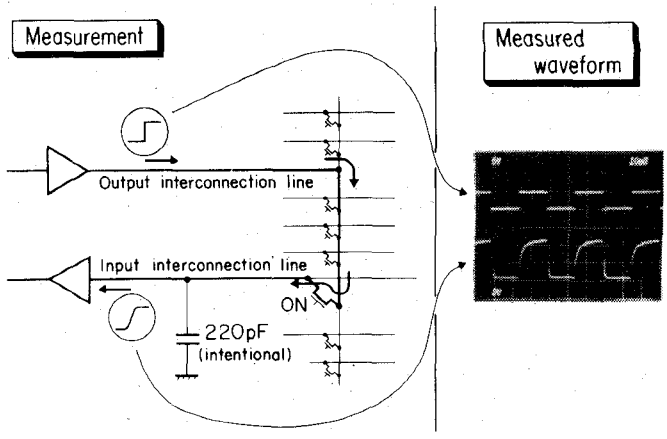

Fig. 6. Transmitted signal waveform that appeared on the input interconnection line with 220-pF capacitive load.

IV. Future Design

An advanced version of this VLSI can be fabricated, using triple-layer polysilicon and double-layer Al, with a 2-μm rule CMOS process. It has on-chip decoder circuits with a high-voltage generator from a single 5-V power-supply voltage for WRITE/ERASE operation on E^2PROM switches. The schematic drawing of the chip design is like the one shown in Fig. 1. It has 60 high-speed CMOS standard logic SSI's/MSI's as functional blocks, which are equivalent to 3K-gate logics, and a 446-row ×233-column switch matrix to enable any combination of input-to-output connection for functional blocks. This chip also offers a logic testing aid. The waveforms at any 16 nodes inside the circuit can be monitored simultaneously. The user can change the monitoring node by designating the ON/OFF switches which let the desired node voltage go out of the chip. Chip size is approximately 10×10 mm. The switch matrix area is 5×7 mm and the functional blocks occupy a 2×7 mm area.

Circuit simulation was carried out to evaluate the speed performance. Fig. 7 shows the model to simulate the propagation delay of the signal, which transmits from one of the outputs to one of the inputs through the switch matrix area. Here, the following factors were assumed: 1) the output buffer had a gate width of 50 μm formed by a 2-μm CMOS standard process; 2) the ON-state switch cell enabled around a 1-mA current flow; 3) the junction capacitance of an E^2PROM source and drain was 5 fF each; and 4) the parasitic capacitance of the output and input interconnection lines was approximately 100 fF/mm, based on the 2-μm-wide wiring. Fig. 8 shows the simulated waveforms that appeared at the output and the input node in the switch matrix. The figure shows the signal transmission upgoing at the switch node (node *A* in Fig. 7). Downgoing signal was also simulated. The average propagation delay in the switch matrix area was found to be 13 ns for the longest transmission path when there were four fan-outs. This speed can be found to be comparable with, or faster than, the rise time or fall time for the CMOS standard logic IC's with the typical 10–100-pF capacitance at an output pin. This means that the users will be able to

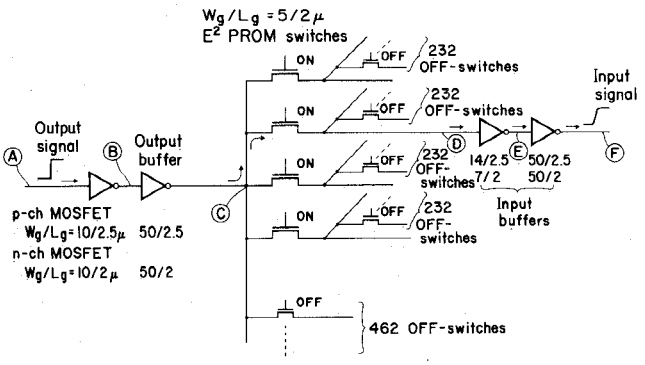

Fig. 7. Model to simulate propagation delay in the switch matrix.

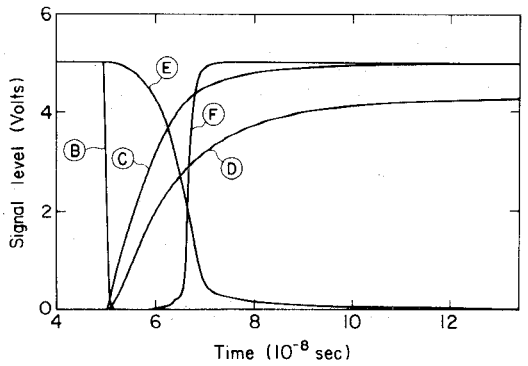

Fig. 8. Simulated signal waveforms at each node when the signal transmits from output to input through switch matrix area. Nodes are represented as *B* through *F*, which are identical to the signs in Fig. 7.

construct a several thousand gate logic system, as if they designed a circuit board using conventional CMOS standard logics.

Further designs of this VLSI include partitioning of the functional block and switch matrix combination to permit more logics available in a chip. With the future 1-μm CMOS process, more than 200 standard logics (equivalent to 10K gates) as functional blocks could be installed in a chip.

V. Conclusion

The proposed new VLSI chip described above provides system and logic designers with a new tool, which makes their system or circuit idea ready to be implemented in the form of an IC and enables prompt debugging and testing of the circuit. The final design is the finishing off for the customized IC fabrication itself, that is, 2- or 3K gate logics (or even more than 10K gates in the future 1-μm design rule era) can be wired in a second to obtain a fully customized IC. The final IC can be completed in less than a day, depending on the ideas involved. An uncustomized "master" IC can be mass-produced and will be reasonably priced. Therefore the personalization can be made, to obtain even a single chip, which means even a single system can be integrated in an IC at reasonable and affordable cost. This innovative VLSI is featured by and can be called "hardware programmable logic IC without process," as opposed to gate arrays, standard cell, and silicon compilers, which require physical and chemical processing, or microprocessor IC's as "software programmable logics."

Acknowledgment

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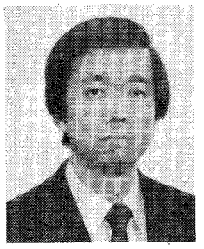

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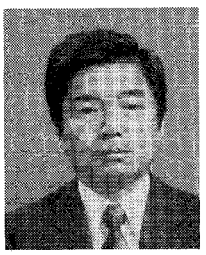

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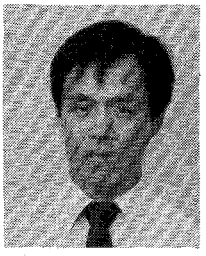

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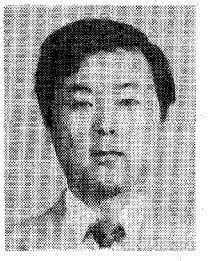

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