A 6K-Gate GaAs Gate Array with a New Large-Noise-Margin SLCF Circuit

TOSHIYUKI TERADA, YASUO IKAWA, MEMBER, IEEE, ATSUSHI KAMEYAMA, KATSUE KAWAKYU, TADAHIRO SASAKI, YOSHIAKI KITAURA, KENJI ISHIDA, KAZUYA NISHIHORI, AND NOBUYUKI TOYODA

Abstract—**A 6K-gate GaAs gate array has been successfully designed and fabricated using a new large-noise-margin Schottky-diode Level-shifter Capacitor-coupled FET logic (SLCF) circuitry and a WN_x-gate self-aligned LDD structure GaAs MESFET process. Chip size was 8.0×8.0 mm^2. A basic cell can be programmed as an SLCF inverter, a two-input NOR, or a two-input NAND gate. The unloaded propagation delay time was 76 ps/gate at a 1.2-mW/gate power dissipation. The increases in delay time due to various loading capacitances were 10 ps/fan-in, 45 ps/fan-out, and 0.64 ps/fF. A 16-bit serial-to-parallel-to-serial (S/P/S) data-conversion circuit was constructed on the gate array as an application example. A maximum operation frequency of 852 MHz was achieved at a 952-mW power dissipation, including I/O buffers.**

I. INTRODUCTION

A LARGE-SCALE gate array approach is one solution used to reduce interchip signal delay and to minimize the development time for new LSI's. GaAs is a candidate for use in a very high-speed gate array because of its small gate delay and low power dissipation. Several GaAs gate arrays have been fabricated, using different kinds of circuitry. Some of them were realized by normally-on logics, BFL [1], [2], and SDFL [3], and others by normally-off logics, DCFL [4], [5], and SBFL [6].

Normally-on logic circuits have a large load driving capability. However, they consume a relatively large amount of power, 2–5 mW/gate, which makes it impossible to realize large-scale (5–10K gate) integration in a chip due to the total power consumption and the resulting cooling requirements.

In contrast, normally-off logic circuits have low-power and high-speed characteristics, and have been thought to be the most promising for LSI's. The noise margin for DCFL or SBFL is, however, too small for reliable operation of GaAs LSI. This is due to the threshold-voltage scattering in a chip, as well as its deviation in a wafer, which relates to material and process limitations.

In response to these circumstances, the authors developed a new circuit, SLCF, which stands for Schottky-diode Level-shifter Capacitor-coupled FET logic [7]. The SLCF circuit has large noise margins and high speed with moderate power dissipation, and has a potential for obtaining higher performance and higher integration with reliable operation than any other circuitry.

This paper describes the basic properties of the SLCF circuit, its application to the design of a 6K gate-array master chip, the fabrication process, and the performance of a basic gate. Application to a 16-bit serial-to-parallel-to-serial data-conversion circuit and its high-speed operation will also be described.

II. SLCF CIRCUIT

The circuit diagram for an inverter, realized by SLCF circuitry, is shown in Fig. 1. It has a switching stage consisting of a load FET and a driver FET, in front of which a level-shift stage, consisting of a Schottky diode and a pull-down FET, is connected. All FET's are normally-on type, and the typical supply voltages are +1.5 V for V_{DD} and −1.0 V for V_{ss}. The main feature of this circuit is created by the Schottky diode in the level-shift stage, which acts not only as a level-shift diode in a dc mode, but also as a feedforward capacitor to accelerate the signal propagation in an ac mode.

In a dc mode, the input signal is level shifted by 0.7 V in the level-shift stage. This avoids the clamping effect in the gate electrode at the next stage, and the potential of the output node at the logic stage varies between 0 V and V_{DD}, resulting in a large logic swing, which is twice as large as that for DCFL, and thus a large noise margin. Fig. 2 shows the simulated result for the noise-margin dependence of the SLCF on the threshold-voltages for load and driver FET's, obtained by using a SPICE simulator. The noise-margin map for DCFL circuitry is also shown in the figure for comparison. The gate widths of 10 μm for both the load and driver FET's in SLCF, and 10 and 20 μm for the load and driver FET's, respectively, in DCFL were considered. The gate length for all FET's was assumed to be 1.5 μm. As is clearly seen in the figure, SLCF has a larger noise margin than DCFL. A 0.2-V noise margin can be provided for a much larger threshold-voltage area than DCFL, and even a 0.4-V noise margin area exists for SLCF, which cannot be obtained in a DCFL circuit.

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The authors are with the VLSI Research Center, Toshiba Corporation, 1, Komukai-Toshiba-cho, Saiwai-ku, Kawasaki 210, Japan.

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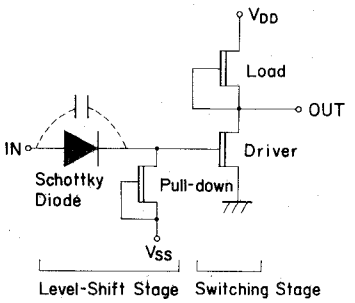

Fig. 1. Circuit diagram for an inverter realized by SLCF circuitry.

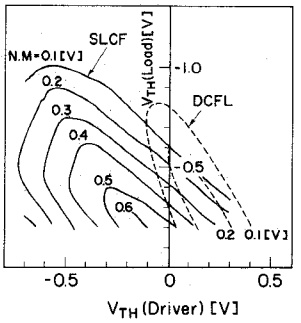

Fig. 2. Simulated noise-margin map for the SLCF as a function of the threshold voltages for the driver and load FET's. DCFL performance is also plotted for comparison.

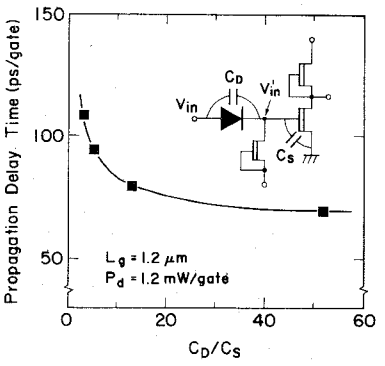

Fig. 3. Propagation delay time dependence on the ratio of C_D to C_S.

In an ac mode, the Schottky diode acts as a feedforward capacitor. The input signal potential at the gate electrode for the driver FET, $V_{in'}$, is given by

$$V_{in'} = \frac{C_D}{C_D + C_s} V_{in} \tag{1}$$

where C_D is the capacitance of the Schottky diode, C_s is the gate-to-source capacitance of the driver FET, and V_{in} is the input signal potential at the IN terminal as shown in Fig. 3. When C_D is large enough to neglect $C_s (C_D \gg C_s)$, $V_{in'}$ becomes nearly equal to V_{in}, meaning that the quick signal transmission is obtained. Fig. 3 shows the measured propagation delay time, obtained from 15-stage ring oscillators using 1.2-μm gate-length FET's, as a function of the ratio of C_D to C_s. Gate widths were 10 μm for both load and driver FET's, and threshold voltages were -0.6 and -0.4 V for load and driver FET's, respectively. The power dissipation was 1.2 mW/gate. The delay time decreased with increasing C_D/C_s ratio, becoming saturated near the $C_D/C_s = 20$ point to reach 70 ps/gate, which is almost the same as for DCFL. This demonstrates that the feedforward capacitor coupling effect of a diode capacitor is effective in maintaining high-speed performance without increasing power consumption.

From these data, it can be concluded that the SLCF circuit ensures reliable operation in LSI level integration because of its large noise margin, while providing high speed and low power dissipation, due to the use of the feedforward coupling effect.

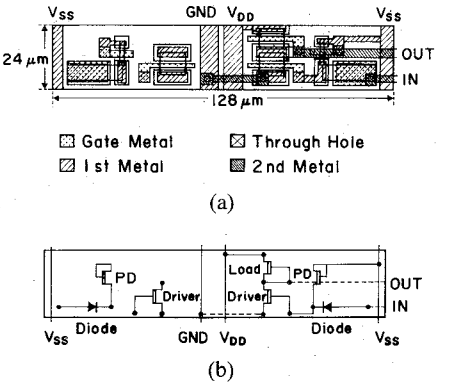

Fig. 4. (a) Pattern layout and (b) equivalent circuit of a basic cell.

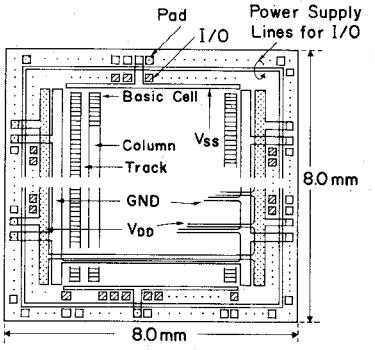

Fig. 5. Schematic drawing of a 6K-gate GaAs gate-array chip.

III. Gate-Array Design

A. Basic Cell

Fig. 4(a) and (b) shows the pattern layout and the equivalent circuit of a basic cell, respectively. It consists of one load FET, two driver FET's, two pull-down FET's, and two Schottky diodes. The gate width/length are 10 μm/1.0 μm for both load and driver FET's. The pull-down FET's were so designed that the current drive should be one-tenth of the load FET, which results in a gate width/length of 2 μm/2.0 μm. The junction area of the Schottky diode is 6×16 μm^2, which is about ten times as large as the gate junction area of the driver FET. In addition, the diode capacitance per unit area is designed to

be three times as large as the driver FET gate-to-source capacitance. Therefore, the ratio of diode capacitance C_D to driver FET gate-to-source capacitance C_s is set at 30, which is large enough to obtain a feedforward effect. The power supply lines in the cell are made of first interconnection metallization, where the 7-μm V_{DD} and ground lines run at the center of each cell, and the 4-μm V_{ss} lines for the level-shift stage are placed in the peripheral area. The size of one basic cell is 128×24 μm^2. A basic cell can be personalized to be one of three circuits, an SLCF inverter, a two-input NOR, or a two-input NAND gate, using three masks, i.e., first/second interconnections and a throughhole. Personalization for an inverter is illustrated in Fig. 4.

B. Chip Design

Fig. 5 shows a schematic drawing of a 6K-gate gate-array chip. Chip size is 8.0×8.0 mm^2. There are 26 columns and each column has 232 basic cells, totaling 6032 cells on a chip.

Between columns, a channel with 21 first-level interconnection lines with a 2-μm design rule for both line and space is provided. Three second-level interconnection lines, with a 3-μm design rule, can run across each basic cell. The minimum throughhole size is 2×2 μm^2.

Surrounding the array region are V_{DD} and ground *GND* main lines, 184 I/O buffers, and 204 pads. Power supply lines for I/O buffers are provided independently from the cell array. An I/O cell is able to be personalized as either an input or an output buffer for a Si-ECL and GaAs-SLCF interface.

IV. Fabrication Process

A. LDD Structure FET

The gate array was fabricated by using a refractory tungsten nitride (WN_x) gate self-aligned MESFET process [8]. In order to realize a high-performance FET, shrinking the gate length is essential to obtain large transconductance and small gate capacitance. In the conventional self-aligned structure FET, however, so-called "short-channel effects" appeared at around 1.5-μm gate length, making further shrinking of the gate length impossible. The short-channel effects were analyzed by using a two-dimensional device simulator, and it was determined that the short-channel effects are mainly caused by the potential lowering in the semi-insulating GaAs substrate beneath the FET channel layer, and are strongly affected by the depth and the spacing of the source/drain n^+ layers.

In order to avoid the potential lowering for suppressing the short-channel effects, a lightly doped drain (LDD) structure was introduced. Fig. 6 shows a cross-sectional illustration of the LDD structure MESFET. The deep and heavily doped n^+ layers, whose junction depth was 0.4 μm, were separated from the gate metal by 0.3-μm-long

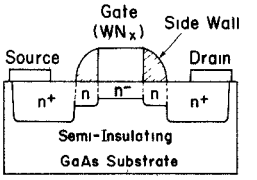

Fig. 6. Cross-sectional illustration of an LDD structure GaAs MESFET.

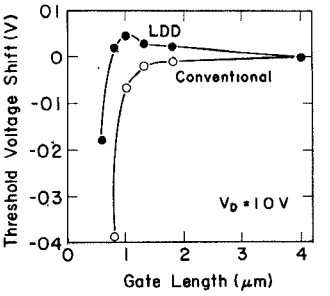

Fig. 7. Threshold-voltage dependence on gate length for LDD and conventional structure FET's.

sidewalls. The moderately doped n layers, whose junction depth was as shallow as 0.12 μm, were placed between the channel n^- layer and deep n^+ layers in order to reduce the series resistance. Fig. 7 shows the short-channel effect in the LDD MESFET, compared with the conventional structure FET. The horizontal axis shows the gate length, and the vertical axis shows the threshold-voltage shift from that of a 4-μm gate-length FET. In the conventional FET, the threshold-voltage shift started at around 1.5-μm gate length, and reached 400 mV at 0.8 μm. The threshold-voltage shift in the LDD FET, on the other hand, was less than 100 mV even at 0.8-μm gate length. Thus it can be concluded that the short-channel effect is remarkably suppressed by using the LDD structure. Consequently, the 1.0-μm gate-length FET was introduced for the gate-array fabrication.

B. Process Conditions

The fabrication process conditions for the gate array were as follows. Channel n^- layers were formed by $^{28}Si^+$ selective implantation into undoped semi-insulating 3-in-diameter LEC GaAs wafers. The acceleration energy was 50 keV, and the dosages were 2.2×10^{12} and 2.8×10^{12} cm^{-2} for driver and load/pull-down FET's, respectively. The active layer of the Schottky diode was formed by double implantation under these conditions to obtain large junction capacitance. Post-implantation annealing was performed at 850°C for 15 min in an $Ar+AsH_3$ mixed atmosphere without any encapsulating film. The WN_x film was deposited by reactive RF magnetron sputtering in $Ar+N_2$ mixed gas. Source/drain n and n^+ layers were formed by $^{28}Si^+$ implantation at 80 keV with a dose of 7×10^{12} cm^{-2} for the n layer and at 180 keV with a dose of 3×10^{13} cm^{-2} for the n^+ layer. Post n^+ implantation anneal was performed at 800°C for 30 min with the PSG film as an encapsulant. The ohmic metal was AuGe/Au.

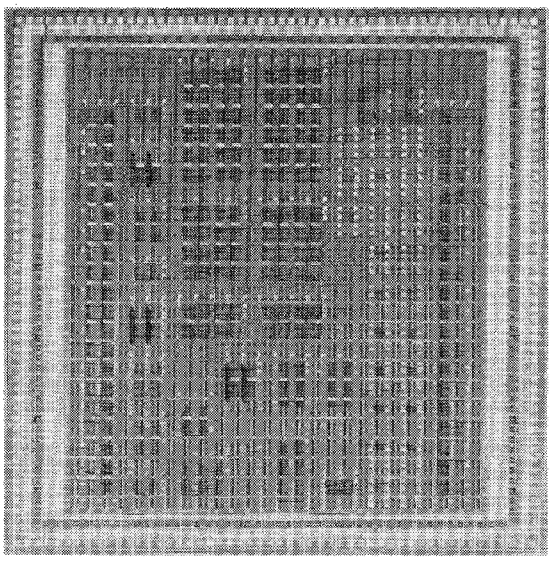

Fig. 8. Photomicrograph of a 6K-gate GaAs gate-array chip on which several test circuits are constructed.

First- and second-interconnection metallizations were Ti/Pt/Au. The Au film thickness differed between the first (0.4 μm) and the second (1.0 μm) levels, resulting in sheet resistivities of $\rho_s = 0.07\ \Omega/\square$ for the first level and $\rho_s = 0.03\ \Omega/\square$ for the second level. The interlayer insulating film was 0.6-μm-thick SiO_2.

V. Basic Gate Performance

In order to evaluate the performance of the gate array, several test circuits were constructured on the chip. Propagation delay time dependence on the kinds of loads was calculated by using the measured data from six different 15-stage ring oscillators. The toggle frequency was measured by using a 1/4 divider implemented by edge-triggered flip-flops. The chip photomicrograph with the test circuits is shown in Fig. 8.

Threshold voltages for the load and driver FET's were -0.7 and -0.45 V, respectively. The K value for the driver FET was measured to be 1.3 mA/V^2 ($W_g = 10\ \mu$m), and the typical transconductance value for the driver FET was 220 mS/mm. The noise margin for a simple SLCF inverter was measured to be 0.3 V, which is large enough to ease constraints as to threshold-voltage deviation.

The results obtained for propagation delay time dependence on loads are as follows. The unloaded (fan-in = fan-out = 1) delay time was 76 ps/gate and the delay time increased at a rate of 10 ps/fan-in, 45 ps/fan-out, and 0.64 ps/fF at a power dissipation of 1.2 mW/gate. If the parasitic capacitance for the 1-mm interconnection line length is assumed to be 70 fF/mm based on the previously reported analytical result [4], which agrees very well with the numerically calculated value reported elsewhere [9], it can be said that the interconnection line load causes a 45-ps/mm additional delay.

The loaded propagation delay time is important rather than the unloaded delay time when actual IC's are fabricated on a gate array. The loaded propagation delay time is empirically given by

$$t_{pd} = t_{pd0} + (I-1)\cdot\Delta t_{pdFI} + (F-1)\cdot\Delta t_{pdFO} + L\Delta t_{pdL} \quad (2)$$

where

- t_{pd0} unloaded ($FI = FO = 1$) propagation delay time,
- Δt_{pdFI} increase in delay time per fan-in,
- Δt_{pdFO} increase in delay time per fan-out,
- Δt_{pdL} increase in delay time per unit interconnection line length,
- I, F number of fan-ins and fan-outs, and
- L interconnection line length.

If the average loading condition is postulated to be fan-in = 1, fan-out = 3, and interconnection line length = 2 mm (140 fF), which is similar to the loading conditions used for Si ECL and Si CMOS gate arrays, the loaded delay time becomes 256 ps/gate.

The 1/4 divider, which was constructed from two edge-triggered flip-flops using 19 cells, operated at 870-MHz typical toggle frequency. The power consumption was 25 mW.

The gate-array performance is summarized in Table I.

TABLE I
6K-Gate GaAs Gate-Array Performance

Chip size	8.0mm x 8.0mm
Circuitry	SLCF
Basic cell size	128μm x 24μm
Number of basic cells	6032 (232 row x 26 column)
Number of I/Os	184 (max.)
Number of pads	204 (including I/O)
Power supply	+1.5 V, -1.0 V
Device size	10μm/1.0μm load & driver FETs 2μm/2.0μm pull-down FET 6μm x 10μm Schottky diode
Design rule for interconnection	
1st level	2μm (width & space)
2nd level	3μm (width & space)
Through hole	2μm x 2μm
FET performance (measured)	
Vth	-0.45 V (driver FET) -0.70 V (load FET)
K-value	1.3 mA/V^2 (Wg=10μm)
Propagation delay time	
Unloaded(fan-out=1)	76 ps/gate
Dependence on load	10 ps/Fan-in 45 ps/Fan-out 45 ps/mm
Power dissipation	1.2 mW/gate

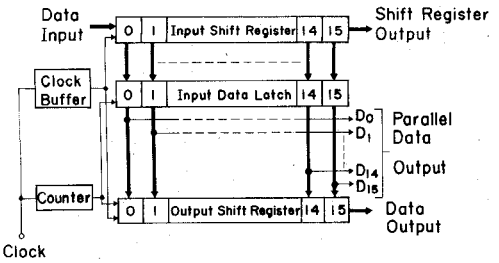

Fig. 9. Logic diagram for a 16-bit S/P/S circuit.

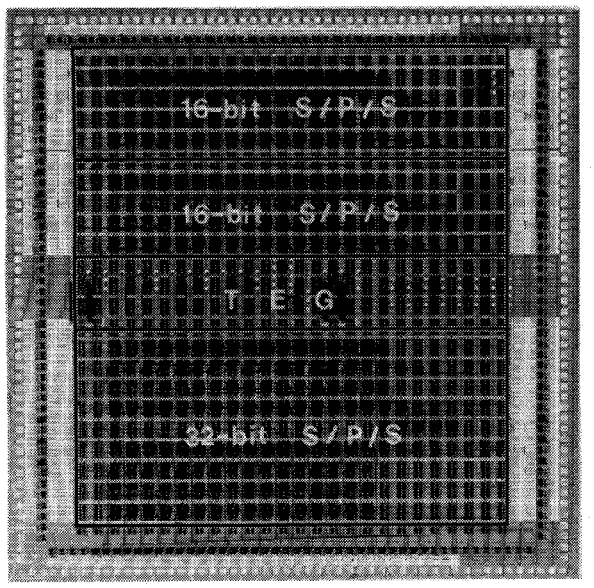

Fig. 10. Photomicrograph of a 6K-gate GaAs gate-array chip, applied to S/P/S circuits.

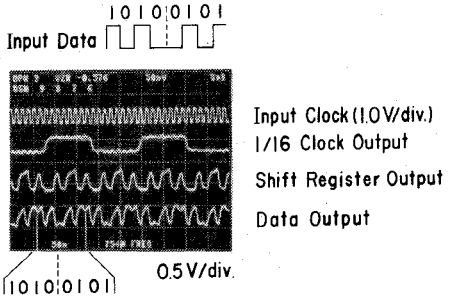

Fig. 11. Input waveform for input clock and output waveforms for counter circuit (1/16 clock output), input serial shift register (shift-register output), and S/P/S converted data (data output). The input pattern is 10100101. The clock frequency is 754 MHz and total power dissipation is 875 mW.

VI. Application

In order to demonstrate the high-speed performance of the gate array, a 16-bit serial-to-parallel-to-serial (S/P/S) data-conversion circuit was designed and fabricated on the gate array as an application example. Fig. 9 shows the logic diagram consisting of a 16-bit serial input register, a 16-bit parallel latch, a 16-bit serial output register with multiplexers, a counter circuit, and a clock driver. This circuit is constructed from 38 edge-triggered flip-flops, 16

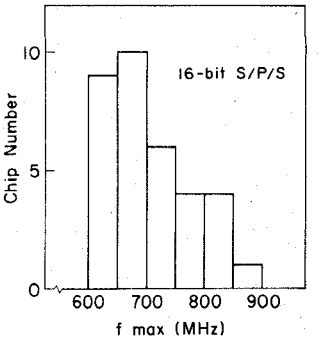

Fig. 12. Distribution of the maximum clock frequency f_{max} for 16-bit S/P/S circuits.

latches, 15 two-input multiplexers, 110 NOR gates, and 22 I/O buffers. It operates as a 16-bit serial shift register, a 16-bit serial-to-parallel data-conversion circuit, and a 16-bit S/P/S data-conversion circuit at the same time. Fig. 10 shows a photomicrograph of the fabricated gate-array chip, on which two 16-bit S/P/S circuits, one 32-bit S/P/S circuit, and a test element group (TEG) were constructed. One 16-bit S/P/S circuit used 579 basic cells and occupied approximately 20 percent of the gate-array area. For a 32-bit S/P/S circuit, 1011 basic cells were used and approximately 40 percent of the area was occupied.

High-speed testing was performed directly on a wafer using a 50-Ω measurement system. Fig. 11 shows an example of test results for a 16-bit S/P/S circuit at a 754-MHz clock frequency. The input data pattern was 10100101, and the waveforms for the input clock, the output data of the counter circuit (1/16 clock), the output data of the serial-input shift register, and the output data of the serial-output shift register are shown in Fig. 11. Power dissipation was 689 mW for the S/P/S data-conversion function block and 186 mW for I/O buffers. Fig. 12 shows the distribution of the maximum operation frequency f_{max} in the measured chips. This circuit operated typically up to 700 MHz and the maximum clock frequency found among the measured chips was 852 MHz, where power consumptions were 745 mW for the internal circuits and 207 mW for the I/O buffers. This speed indicated that the gate delay time for the critical path inside the circuit was 220 ps/gate, which approximately agreed with the simulated result by using the measurement data obtained from the ring oscillators as mentioned previously.

VII. Conclusion

A 6K-gate GaAs gate array was developed by using the newly developed SLCF circuitry, which ensures reliable operation in LSI level integration because of its large noise margin, while using the feedforward coupling effect to provide high speed and low power dissipation. A basic cell can be programmed as an SLCF inverter, a two-input NOR, or a two-input NAND gate. A 1.0-μm WN_x-gate self-aligned LDD structure MESFET process was adopted to fabricate this gate array, in order to obtain a high-performance FET by shrinking the gate length while suppressing the short-

channel effects. The basic performances for this gate array were evaluated by several test circuits. The unloaded delay time was 76 ps/gate at a 1.2-mW/gate power dissipation, and the increases in delay time due to loading capacitances were 10 ps/fan-in, 45 ps/fan-out, and 0.64 ps/fF, resulting in a loaded propagation delay time of 256 ps/gate under the condition of three fan-outs and 2-mm interconnection line length. A 16-bit S/P/S data-conversion circuit was constructed on the gate array as an application example, and the maximum operation frequency of 852 MHz was achieved at a 952-mW power consumption, including I/O buffers.

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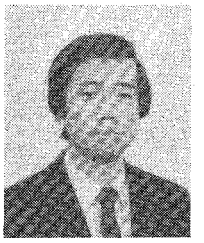
Toshiyuki Terada received the B.E. degree in electrical engineering from Tohoku University, Sendai, Japan, in 1981.

In 1981 he joined the Toshiba Research and Development Center. He has been engaged in the research and development of GaAs digital IC's and is working on GaAs device technology. He is presently a Technical Staff Member at Toshiba VLSI Research Center, Kawasaki, Japan.

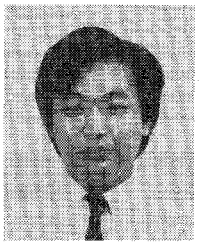
Mr. Terada is a member of the Institute of Electronics, Information and Communication Engineers of Japan, and the Japan Society of Applied Physics. In 1985 he received the Beatrice Winner Award for Editorial Excellence for his co-authored paper entitled "42ps 2K-Gate GaAs Gate Array with a WN Self-Aligned FET Process," presented at the IEEE 1985 International Solid-State Circuits Conference.



Yasuo Ikawa (M'81) was born in Japan on May 16, 1949. He received the B.E. and M.E. degrees in electronics, both from Tokyo Institute of Technology, Tokyo, Japan, in 1973 and 1975, respectively.

In 1975 he joined the Toshiba Research and Development Center, Kawasaki, Japan, where he was doing research on silicon ribbon solar cells and GaAs devices including their digital applications. From October 1980 to April 1982 he worked with Prof. R. W. Dutton as a Visiting Research Associate at the Integrated Circuits Laboratory, Stanford Electronics Laboratories, Stanford University, Stanford, CA, where he worked on characterization and modeling techniques for high-speed integrated circuits. After returning to Japan, he was involved in the development of GaAs digital IC's at the Toshiba Research and Development Center, and then at Toshiba VLSI Research Center, as a Researcher in charge of GaAs IC design and device technologies. In October 1986 he was appointed Deputy Manager for the Planning Group at Toshiba Research and Development Center. His current interests focus on GaAs digital IC's and IC design methodology as well as microelectronics in general.

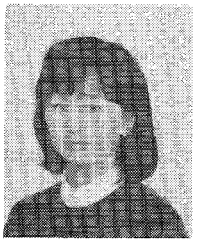
Mr. Ikawa is a member of the Institute of Electronics, Information and Communication Engineers of Japan and the Japan Society of Applied Physics. In 1985 he received the Beatrice Winner Award for Editorial Excellence for his co-authored paper entitled "42 ps 2K-Gate GaAs Gate Array with a WN Gate Self-Aligned FET Process," given at the IEEE 1985 International Solid-State Circuits Conference.



Atsushi Kameyama was born in Hyogo Prefecture, Japan, on February 22, 1959. He received the B.S. and M.S. degrees in physical electronics from Tokyo Institute of Technology, Tokyo, Japan, in 1982 and 1984, respectively.

In 1984 he joined the Toshiba VLSI Research Center, Kawasaki, Japan. He has been engaged in the circuit design and development of GaAs digital IC's.

Mr. Kameyama is a member of the Institute of Electronics, Information and Communication Engineers of Japan.



Katsue Kawakyu received the B.E. degree in electrical engineering from Tohoku University, Sendai, Japan, in 1981.

In 1981 she joined the Toshiba Research and Development Center. She has been engaged in the research and development of GaAs digital IC's. She is presently a Technical Staff Member at Toshiba VLSI Research Center, Kawasaki, Japan, working on GaAs digital IC design.

Ms. Kawakyu is a member of the Institute of Electronics, Information and Communication Engineers of Japan. In 1985 she received the Beatrice Winner Award for Editorial Excellence for her co-authored paper entitled "42ps 2K-Gate GaAs Gate Array with a WN Self-Aligned FET Process," presented at the IEEE 1985 International Solid-State Circuits Conference.

Tadahiro Sasaki received the M.Sc. degree in physics from Nihon University, Tokyo, Japan, in 1985.

In 1985 he joned the Toshiba VLSI Research Center, Kawasaki, Japan, where he has been engaged in the research and development of GaAs digital IC's.

Mr. Sasaki is a member of the Institute of Electronics, Information and Communication Engineers and Physical Society of Japan.

Yoshiaki Kitaura was born in Osaka, Japan, on December 1, 1958. He received the B.E. degree in metallurgical engineering from the National University of Yokohama in 1982.

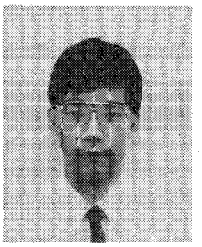
In 1982 he joined the Toshiba Research and Development Center, Toshiba Corporation, Kawasaki, Japan, where he has been engaged in the research and development of GaAs devices. His research interests are mainly in the process technology of self-aligned gate GaAs MESFET. He is presently a Technical Staff Member at Toshiba VLSI Research Center.

Mr. Kitaura is a member of the Japan Society of Applied Physics. In 1985 he received the Beatrice Winner Award for Editorial Excellence for his co-authored paper entitled "42 ps 2K-Gate GaAs Gate Array with a WN Gate Self-Aligned FET Process," presented at the IEEE 1985 International Solid-State Circuits Conference.

Kenji Ishida was born in Japan on April 29, 1958. He received the B.E. and M.E. degrees in electronic engineering from Toyohashi University of Technology, Toyohashi, Japan, in 1981 and 1983, respectively.

In 1983 he joined the Toshiba Research and Development Center, Toshiba Corporation, Kawasaki, Japan, where he has been engaged in the research and development of GaAs devices. He is presently a Technical Staff Member at the Toshiba VLSI Research Center.

Mr. Ishida is a member of the Institute of Electronics, Information and Communication Engineers of Japan and the Japan Society of Applied Physics.



Kazuya Nishihori received the B.S. degree in physics from the University of Tokyo, Tokyo, Japan, in 1984.

In 1984 he joined the Toshiba Research and Development Center, Kawasaki, Japan. He has worked on the research and development of GaAs digital IC's.

Mr. Nishihori is a member of the Japan Society of Applied Physics.

Nobuyuki Toyoda received the B.E., M.E., and Ph.D. degrees in electronic engineering from Waseda University, Tokyo, Japan, in 1971, 1973, and 1978, respectively.

He worked on liquid-phase epitaxial growth of GaAs, ion-implantation in GaAs, development of GaAs varactor and mixer diodes, GaAs Hall devices, and GaAs FET at Matsushita Research Institute, Tokyo, Japan, beginning in 1973. In 1980 he joined Toshiba Research and Development Center, Kawasaki, Japan, where he has been engaged in the development of GaAs high-speed logic IC's. He is presently a Researcher responsible for GaAs digital IC research and development at the Toshiba VLSI Research Center.

Dr. Toyoda is a member of the Japan Society of Applied Physics. In 1985 he received the Beatrice Winner Award for Editorial Excellence for his co-authored paper entitled "42 ps 2K-Gate GaAs Gate Array with a WN Gate Self-Aligned FET Process," presented at the IEEE 1985 International Solid-State Circuits Conference.