Nondestructive Readout of Ferroelectric-Gate Field-Effect Transistor Memory With an Intermediate Electrode by Using an Improved Operation Method

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***Abstract*—We investigated the reading and writing of ferroelectric-gate field-effect transistor memory with an intermediate electrode (IF-FET) to achieve perfect nondestructive readouts. In the previous operation method, although the difference in output voltage $\Delta V_{\rm O}$ between positive $(P_{\rm r}^{+})$ and negative $(P_{\rm r}^{-})$ remanent polarization memory states was adequate for the first reading time, the nondestructive readout for the $P_{\rm r}^{-}$ state was seriously degraded due to the generation of nonreturning domains. In order to solve this issue, a $P_{\rm r}^{0}$ memory state was used instead of the previous $P_{\rm r}^{-}$ memory state. The $P_{\rm r}^{0}$ state was induced by applying a pulse combined with a positive voltage $(V_{\rm W}^{+})$ and a negative voltage $(V_{\rm W}^{-})$. $V_{\rm W}^{+}$ was to reset the previously written memory states, and $V_{\rm W}^{-}$ was to control the amount of remanent polarization. In addition, in order to extinguish perfectly the nonreturning domains, a negative voltage $V_{\rm R}^{-}$ was applied for data reading, following a positive voltage $V_{\rm R}^{+}$, where $V_{\rm R}^{+}$ was determined for clear decoding. The appropriate heights of the writing and reading voltages were determined individually from the viewpoint of good nondestructive readout and large $\Delta V_{\rm O}$. As a result, it was verified experimentally that the reading endurance reached more than 10^{8} cycles and that the retention time of IF-FET at 150 °C was possible to exceed ten years.**

***Index Terms*—Ferroelectric gate, ferroelectric memory, nondestructive readout, reading endurance, retention.**

I. Introduction

FERROELECTRIC-GATE field-effect transistor memory (F-FET) is well known as one of the ultimate nonvolatile memories because of its remarkable features such as nondestructive readout, high packing density, high reading speed, and low power consumption [1]–[3] compared with 1-transitor–1-capacitor (1T–1C) or 2-transistor–2-capacitor (2T–2C) ferroelectric random access memories (FeRAMs). Furthermore, it has advantages of low writing voltage, fast writing speed, and high endurance compared with flash memory [4]–[6]. In recent years, considerable research has been carried out on F-FET [7]–[11], but it has not been commercialized so far due to the following serious problems. First, due to an insulating buffer layer which must be inserted to prevent chemical reaction between the ferroelectric film and the Si substrate [12], [13], the ferroelectric film is subjected to a depolarization field even under a retention condition of zero bias between the ferroelectric gate and the Si substrate [14], [15]. This depolarization field is caused by the charges which are induced on the insulating buffer layer by the remanent polarization of the ferroelectric film. The depolarization field makes the remanent polarization of the ferroelectric film relax, leading to a short retention time [16], [17]. The second problem is high writing voltage due to the voltage drop on the buffer layer [5], [18]. To reduce the voltage drop, a high dielectric constant material (high-k material) is normally employed. Unfortunately, the interface between the high-k material and the Si substrate is poor, which leads to an unstable memory performance. In order to overcome these problems, Shimada *et al.* [19] has proposed a new operational principle of F-FET memory, in which an intermediate electrode for data writing is inserted between the ferroelectric gate and the buffer layer. This F-FET memory is denoted as IF-FET, and its features have been reported in detail elsewhere [20], [21]. Fig. 1 shows a schematic drawing of IF-FET, which consists of a ferroelectric capacitor $(C_{\rm f})$ in serial connection with a MOSFET. The input capacitance is denoted as $C_{\rm i}$. For data writing, a voltage $V_{\rm W}$ as writing pulse is applied directly to the only $C_{\rm f}$, using the top and intermediate electrodes. The remanent polarization of $C_{\rm f}$ is set positive $(P_{\rm r}^{+})$ for $V_{\rm W} > 0$ or negative $(P_{\rm r}^{-})$ for $V_{\rm W} < 0$. For data reading, with the intermediate electrode being electrically floated, a positive reading voltage $V_{\rm R}$ as reading pulse is applied between the top electrode and the ground or source of the MOSFET, where $C_{\rm f}$ is connected in series with the gate of the MOSFET. By measuring the output voltages $V_{\rm O}$'s on a resistor R, the memory states can be decoded, where the biased voltage to the drain is $V_{\rm D}$ through R. The MOSFET acts as a reading transistor for this memory. In general, $C_{\rm f}$ from the $P_{\rm r}^{+}$ state is much smaller than $C_{\rm f}$ from the $P_{\rm r}^{-}$ state when $C_{\rm f}$ is applied by a positive voltage. Here, we define the ferroelectric capacitances from the $P_{\rm r}^{+}$ and $P_{\rm r}^{-}$ states as $C_{\rm fl}$ and $C_{\rm fh}$, respectively. Using a small $C_{\rm fl}$, the intermediate voltage $V_{\rm I}$ to the ground can be lower than the threshold voltage $V_{\rm th}$ of the MOSFET or the reading transistor, so that the transistor is set OFF state or that the output voltage characteristics are flat, as shown in Fig. 1. Also, using a large $C_{\rm fh}$, $V_{\rm I}$ can be higher than $V_{\rm th}$, so that the transistor is set ON state and that the drain current $I_{\rm D}$ flows. As a result, the output voltage characteristics are pulse trains. From this operational principle, using IF-FET with the intermediate electrode, the operation voltage can be

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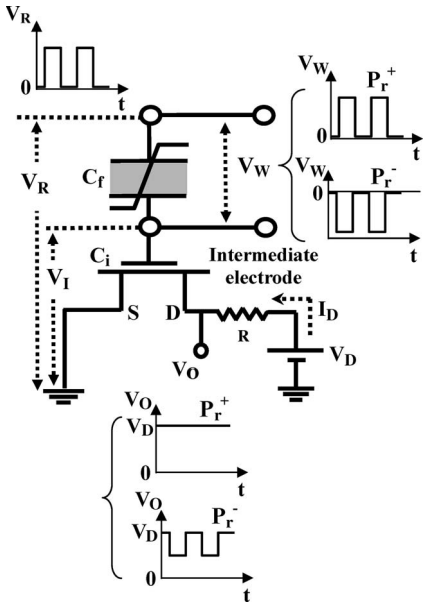

Fig. 1. Operation principle of IF-FET memory.

lowered not only because the writing voltage is applied only to the ferroelectric capacitor but also because a high reading voltage to saturate the polarization of ferroelectric capacitor like FeRAM is not needed. Owing to this, silicon oxide can be used as a buffer layer or gate instead of high-k material, which leads to an excellent interface property with Si to obtain stable device operation. Additionally, the remanent polarization of the memory states can be protected under zero-bias condition, so that the retention time extends much longer.

So far, we used $P_{\rm r}^{+}$ and $P_{\rm r}^{-}$ remanent polarizations as memory states, and a positive unipolar square pulse was applied for data reading. Although the difference in output voltage $\Delta V_{\rm O}$ between $P_{\rm r}^{+}$ and $P_{\rm r}^{-}$ memory states was adequate for the first reading, $\Delta V_{\rm O}$ decreased with the reading cycle. It has been demonstrated that the reading endurance of IF-FET memory reaches to 10^{6} cycles [22], which is much smaller than that of 10^{12} cycles for FeRAM. In particular, for the $P_{\rm r}^{-}$ state, $V_{\rm O}$ degraded very fast with the reading cycle. This is because all of the downward domains switched by reading out from the upward domains of the initial $P_{\rm r}^{-}$ state do not return to the initial upward states, and some domains still remain downward in the read-out $P_{\rm r}^{-}$ state. These domains, which are called nonreturning domains as reported before [21], make the nondestructive readout of the $P_{\rm r}^{-}$ state degraded. For this issue, Shimada *et al.* used a low reading voltage without polarization reversal of the $P_{\rm r}^{-}$ state. However, since the low reading voltage leads to a lower output voltage than that of conventional destructive readout FeRAMs, the operation easily fails due to degradation in ferroelectric properties such as the imprint phenomenon. In our case, however, a high-enough voltage for readout is used, which leads to destructive readout without failure.

In order to solve this issue, first, we used a memory state $P_{\rm r}^{0}$ instead of a $P_{\rm r}^{-}$ state to reduce the amount of nonreturning domains. The $P_{\rm r}^{0}$ memory state was proposed also by Shimada *et al.* [23], [24]. The ideal state of the $P_{\rm r}^{0}$ state is nonpolarized in $C_{\rm f}$. They used the state to minimize the imprint effect in 2T–2C FeRAMs and, essentially, for nondestructive readout. Second, for data reading, we proposed a new combined reading pulse of a negative voltage $V_{\rm R}^{-}$ following a positive voltage $V_{\rm R}^{+}$. While $V_{\rm R}^{+}$ produces a sufficient output voltage for decoding, $V_{\rm R}^{-}$ plays a role to return the nonreturning domains to the initial state, i.e., to recover the memory state. The effectiveness of our new operating method on nondestructive readout has already been reported roughly [25]. The report, however, does not mention the details of the operation principle and the determination process of operation parameters, e.g., $V_{\rm R}^{+}$ and $V_{\rm R}^{-}$. Furthermore, other memory characteristics such as reading endurance and retention time have never been reported so far.

In this paper, at first, we explain the origin of the issue on nondestructive readout and present our original method to solve it, i.e., using the $P_{\rm r}^{0}$ memory state and the combined reading pulse, in detail. Next, we present and discuss the experimental results to investigate the operation parameters of the method for nondestructive readout. Finally, using the appropriate conditions, we show, for the first time, the results of reading endurance and retention characteristics under almost perfectly nondestructive readouts compared with those of the previous memory state and reading pulse.

II. Improvement

A. Origin of the Issue

In the previous operation method, $V_{\rm W}$'s with two square pulses, e.g., of $+4$ or -4 V, were applied to produce the memory state of $P_{\rm r}^{+}$ or $P_{\rm r}^{-}$, respectively. For data reading, $V_{\rm R}$'s with two positive unipolar square pulses, e.g., of 3.5 V, were applied. Fig. 2(a) and (b) shows the dependences of the output voltage of the $P_{\rm r}^{+}$ state, $V_{\rm O}(P_{\rm r}^{+})$, and that of the $P_{\rm r}^{-}$ state, $V_{\rm O}(P_{\rm r}^{-})$, for the first, second, and tenth reading times. The read-out memory state after each reading out, from the first to the tenth time, was retained for 1 min under the condition that the intermediate electrode was electrically floated and that the top electrode and both the source and drain of the reading transistor were grounded. From Fig. 2, it can be seen that $V_{\rm O}(P_{\rm r}^{+})$ measured as $V_{\rm O}^{n}(P_{\rm r}^{+})$ after the nth readout does not vary and has a constant value of $V_{\rm D} = 2$ V. This memory state is nondestructive. However, $V_{\rm O}^{n}(P_{\rm r}^{-})$ of $V_{\rm O}(P_{\rm r}^{-})$ at the nth reading time increases with n and approaches $V_{\rm D}$, which means that this memory state is gradually changed close to $P_{\rm r}^{+}$ and that the two memory states become hardly distinguishable. This is due to the generation of nonreturning domains as mentioned before.

Fig. 3 shows the schematic drawings of the ferroelectric domains in $C_{\rm f}$ and stored charges on the equivalent circuits of $C_{\rm f}$ connected in series with an input capacitor $C_{\rm i}$ of the reading transistor for the previous reading-out process of the $P_{\rm r}^{-}$ memory state. Fig. 3(a)–(d) is for the initial memory state, during the reading-out operation, just after the reading out, and in a nearly steady state after the reading out, respectively. At the top of the figure, the reading pulses are schematically drawn for the (a)–(d) conditions, indicating each operation point as an individual dot. The remanent charge $-Q_{\rm f} < 0$ is stored as an initial memory state of $P_{\rm r}^{-}$, as shown in Fig. 3(a). A charge $\Delta Q > 0$ is induced by applying a positive $V_{\rm R}$ to the serial capacitance of $C_{\rm f}$ and $C_{\rm i}$, as shown in Fig. 3(b), since some of

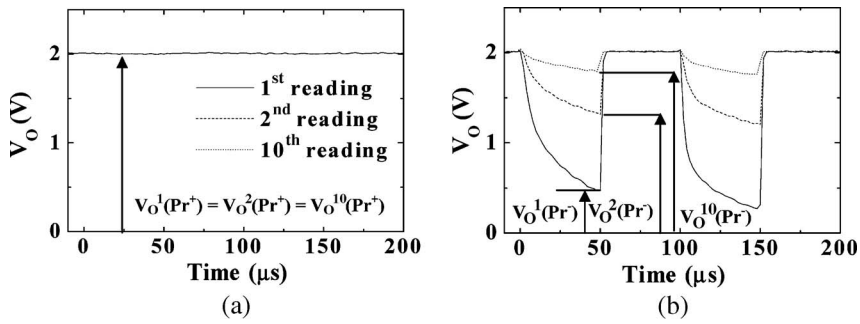

Fig. 2. Readout characteristics of the first, second, and tenth readings, which were measured with the previous operation method. (a) For the P_r^+ state. (b) For the P_r^- state.

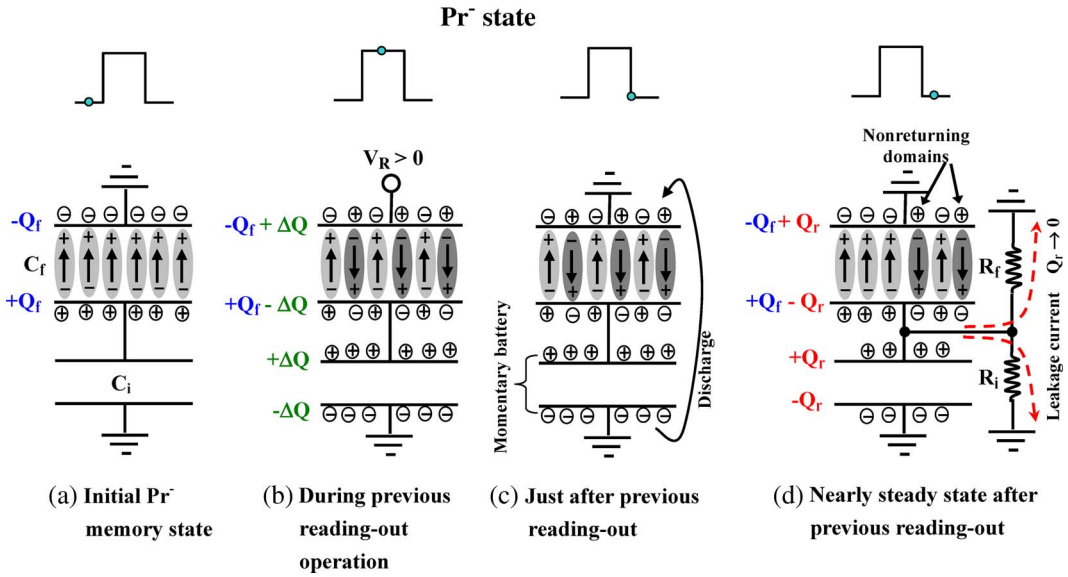

Fig. 3. Schematic drawings of ferroelectric domains in C_f and stored charges on serially connected capacitances of C_f and C_i for the previous reading-out process of the P_r^- state. (a) Initial P_r^- state, (b) during the reading out, (c) just after the reading out, and (d) nearly steady state after the reading out. At the top of the figure, the reading pulse is drawn for each state, and each operation point is indicated as a dot.

the upward domains in Fig. 3(a) are switched to the downward domains. When V_R falls to zero, ΔQ stored on C_i acts as a momentary battery to C_f, and some amount of ΔQ moves to C_f, as shown in Fig. 3(c). Because the voltage magnitude of the momentary battery is not as large as that of V_W for the P_r^- state, some of the switched domains do not return to the initial upward state, which are nonreturning domains. That is, the ΔQ is reduced but never becomes zero. Thus, on the input capacitance C_i of the reading transistor, some positive charge Q_r remains after each reading out, as shown in Fig. 3(d), where Q_r is called a remaining charge hereafter. Since C_f and C_i have finite huge resistances of R_f and R_i, respectively, leakage current through C_f and C_i flows from the charge source of Q_r so that Q_r on C_i reduces to zero roughly within the time constant, depending on the capacitances and resistances. However, because Q_r on C_f is terminated with ferroelectric polarized domain and is held, it never vanishes, and the initial remanent charge Q_f of the P_r^- state is changed to $-Q_f + Q_r$. Therefore, $V_O^n(P_r^-)$ increases with the reading time, as shown in Fig. 2(b). On the other hand, for the P_r^+ state, there is a small amount of remaining charge on C_i after reading out because most of the domains in this memory state are downward and the domains switched by V_R are few. Moreover, since the reading operation in this state acts as the rewriting operation, the nondestructive readout is performed without failure. Therefore, we can conclude that it is necessary to suppress the generation of nonreturning domains after reading out for the sake of the nondestructive readout of the P_r^- state.

B. *Improvement of Memory State and Reading Pulse*

In order to solve the issue on nondestructive readout of IFFET [25], instead of a P_r^- state, we use a P_r^0 state whose position in the $P-E$ hysteresis loop is not exact but near the origin, as shown in Fig. 4(a). The P_r^0 state can be produced by a combined pulse consisting of a positive part (V_W^+) followed by a negative part (V_W^-), as shown in Fig. 4(b). V_W^+ acts as a reset pulse to the data-written memory cell. Increasing $|V_W^-|$ increases the number of upward domains switched from the downward domains produced by V_W^+, and the magnitude of V_W^- can control a total polarization charge on C_f. In order to suppress the generation of nonreturning domains, $|V_W^-|$ should be reduced to limit the number of upward domains. However, reducing $|V_W^-|$ excessively makes the memory state approach the P_r^+ state, and the difference in V_O between both memory states becomes smaller, which is not favorable for data decoding.

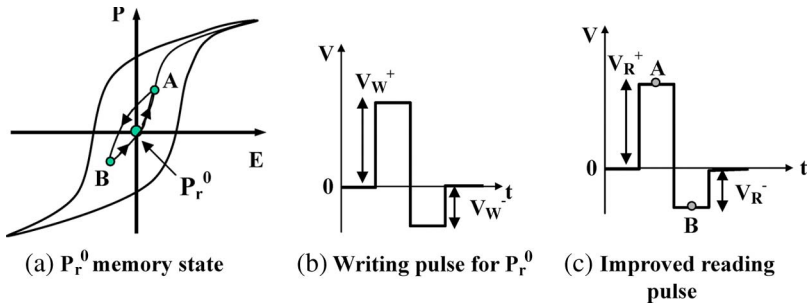

Fig. 4. (a) Schematic major $P-E$ hysteresis loop with a minor loop showing a reading operation trace of the P_{r}^0 state, (b) writing pulse to produce the P_{r}^0 state, and (c) improved reading pulse. Points A and B in (a) correspond to points A and B, respectively, of the improved reading pulse in (c).

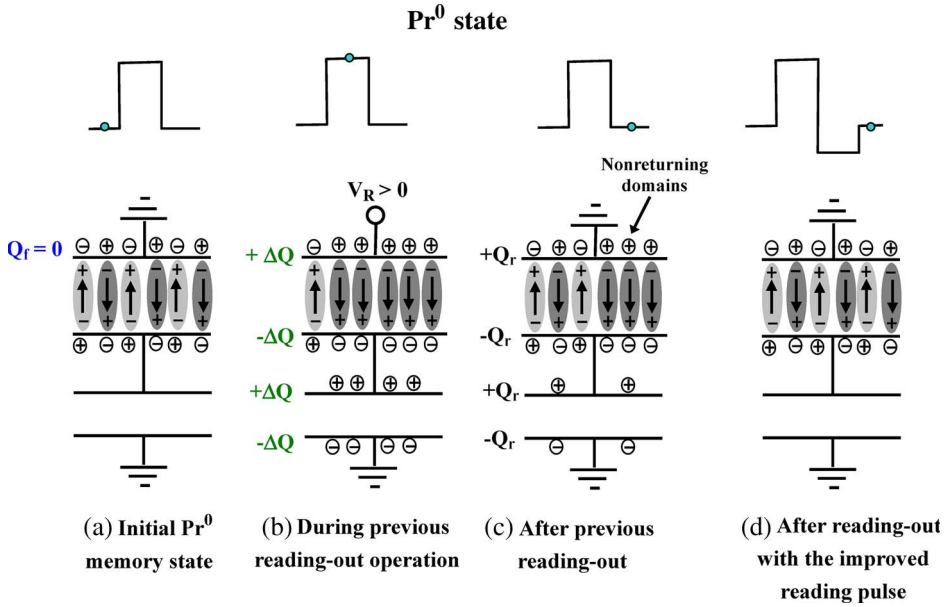

Fig. 5. Schematic drawings of ferroelectric domains in C_{f} and stored charges on C_{f} and C_{i} for the reading-out process of the P_{r}^0 state. (a) Initial P_{r}^0 state, (b) and (c) during and after the reading out with the previous reading pulse, respectively, and (d) after the reading out with the improved reading pulse consisting of a positive voltage and a negative voltage. At the top of the figure, the reading pulse is drawn for each state, and each operation point is indicated as a dot.

Therefore, there is an appropriate $|V_{\mathrm{W}}^-|$, for which the P_{r}^0 state is probably near the origin of $P-E$ hysteresis loop, as shown in Fig. 4(a). Even if the P_{r}^0 state is used, nonreturning domains are still generated as long as the previous reading pulse is used, where the amount after reading out is much smaller compared with that of the P_{r}^- state. These charge states are schematically shown in Fig. 5 (as in Fig. 3). In this case, the P_{r}^0 state is nonpolarized so that the volume of upward domains is equal to that of downward domains. In order to return Q_{r} on C_{i} to C_{f} as the initial memory state, we use a combined reading pulse consisting of a negative V_{R}^- following a positive V_{R}^+, as shown in Fig. 4(c). V_{R}^+ is used for data decoding, and V_{R}^- acts as a rewriting operation for the P_{r}^0 state. The operation points of polarization–voltage $(P-V)$ hysteresis loop corresponding to V_{R}^+ (A) and V_{R}^- (B) in Fig. 4(c) are indicated as dots of A and B, in Fig. 4(a), respectively, and the reading operation traces a minor loop. By using this combined pulse, Q_{r} on C_{i}, as well as on C_{f}, is reduced to zero, and the read-out P_{r}^0 state can return to the initial memory state, as shown in Fig. 5(d), which means that nondestructive readout can be complemented. Here, we notice that $|V_{\mathrm{R}}^-|$ should be small enough in order not to destroy the P_{r}^+ memory state. This is because an excessively large $|V_{\mathrm{R}}^-|$ can switch some amount of downward domains of the P_{r}^+ state to upward domains, and a nonnegligible remaining charge is stored on C_{i} due to nonreturning domains like in the P_{r}^- case. Therefore, there is an appropriate $|V_{\mathrm{R}}^-|$ in the combined reading pulse, where $|V_{\mathrm{R}}^-|$ depends on $|V_{\mathrm{W}}^-|$ which determines the actual P_{r}^0 memory state.

III. Experimental Setup

The discrete circuit based on Fig. 1 was used to determine the appropriate V_{W}^+, V_{W}^-, V_{R}^+, and V_{R}^- for the nondestructive readout of IF-FET memory. The output voltage V_{O} was measured on a resistor of 2 kΩ connected with the drain of the MOSFET, which was biased by a dc voltage V_{D} of 2 V. In this circuit, we used an n-channel commercial MOSFET with $V_{\mathrm{th}} = 1.4$ V and $C_{\mathrm{i}} = 180$ pF. The preparation of C_{f} consisting of (RuO_x top electrode)/ PZT/ (Pt/RuO_x bottom electrode) on the SiO_2/Si substrate was described in our previous report [26]. The ferroelectric layer was a 200-nm-thick and highly (100)/(001)-oriented PZT film. The leakage current density of C_{f} is approximately 10^{-5} A/cm^2 at the applied voltage of ±4 V. Since the ferroelectric property of C_{f} is necessary

to estimate not only the IF-FET performance but also the appropriate writing and reading voltages, $P-V$ measurements of $C_{\rm f}$ were performed using a Sawyer–Tower circuit with a sine wave at 100 Hz. The applied voltage $V_{\rm W}^{+}$ was determined so that it would be not only enough to saturate the polarization of $C_{\rm f}$ but also as low as possible for low-voltage operation. $V_{\rm R}^{+}$ was determined for decoding the memory states more distinctly, in which the intermediate $V_{\rm I}$ nearly became $V_{\rm th}$ of the MOSFET, or $V_{\rm O}(P_{\rm r}^{+})$ hardly responded to the reading pulse and almost kept $V_{\rm D}$. As for $V_{\rm W}^{-}$, at first, from the two viewpoints of suppressing nonreturning domain generation and increasing $\Delta V_{\rm O}=V_{\rm O}(P_{\rm r}^{+})-V_{\rm O}(P_{\rm r}^{-})$, the difference in $V_{\rm O}$ between the $P_{\rm r}^{+}$ and $P_{\rm r}^{-}$ states, we investigated to obtain the appropriate range by using the previous positive reading pulse. Then, both $V_{\rm W}^{-}$ and $V_{\rm R}^{-}$ were determined simultaneously so that a nondestructive readout could be achieved, with $\Delta V_{\rm O}$ being as large as possible. After determining the four appropriate voltages of the writing and reading pulses, the reading endurance was analyzed. The memory states of $P_{\rm r}^{+}$ and $P_{\rm r}^{0}$ were read out continuously up to 10^{8} times by using the combined reading pulse with the frequency of 10 kHz. Also, the retention characteristics were investigated. The two samples of $P_{\rm r}^{+}$ and $P_{\rm r}^{0}$ states were stored at 150 °C in air for a maximum duration of 24 h, and the retention time was estimated by means of an extrapolation method.

IV. Results and Discussion

A. Determination of the Pulse Heights of Writing and Reading Pulses

1) $V_{\rm W}^{+}$ and $V_{\rm R}^{+}$: From the measured hysteresis loop, we obtain the dependences of the twice remanent polarization $2P_{\rm r}$ and of the coercive voltage $V_{\rm c}$ on the voltage applied to the ferroelectric capacitor. By this measurement, $V_{\rm W}^{+}$ was determined to be 4 V, around which $2P_{\rm r}$ and $V_{\rm c}$ began to saturate. For distinct memory operation, the gate voltage of the MOSFET for the $P_{\rm r}^{+}$ memory state, $V_{\rm I}(P_{\rm r}^{+})$ at applying $V_{\rm R}^{+}$ of the combined reading pulse, should be equal to or a little smaller than the threshold voltage of the MOSFET. Since $C_{\rm fl}$ is much smaller than $C_{\rm fh}$ from $P_{\rm r}^{0}$ in general, this criterion for $V_{\rm R}^{+}$ is automatically satisfied for the $P_{\rm r}^{0}$ state, which brings a clear inverse response to the reading pulse.

Using the measured $P-V$ hysteresis loop and the device parameters of the MOSFET, we calculated $V_{\rm R}^{+}=3.5$ V, where $C_{\rm fh}$ and $C_{\rm fl}$ were roughly estimated to be 155 and 104 pF, respectively. Also, we confirmed experimentally that this value of $V_{\rm R}^{+}$ was adequate for memory operation.

2) $V_{\rm W}^{-}$ and $V_{\rm R}^{-}$: Fig. 6 shows $|V_{\rm W}^{-}|$ dependences of $\Delta V_{\rm O}^{1}$ and $\Delta V_{\rm O}^{1-2}(P_{\rm r}^{0})$. $\Delta V_{\rm O}^{1}$ is the difference in $V_{\rm O}$ between the $P_{\rm r}^{+}$ and $P_{\rm r}^{0}$ states at the first reading time, and $\Delta V_{\rm O}^{1-2}(P_{\rm r}^{0})$ is the difference in $V_{\rm O}$ of the $P_{\rm r}^{0}$ state between the first and the second reading time. The 1–2 superscript indicates the reading times of the first to the second. In this case, $V_{\rm W}^{+}=4$ V, $V_{\rm R}^{+}=3.5$ V, and $V_{\rm R}^{-}=0$ which is the previous reading pulse. From this figure, we can see that $\Delta V_{\rm O}^{1}$ increases with $|V_{\rm W}^{-}|$ because $C_{\rm fh}$ which is proportional to the volume of the upward domain increases with $|V_{\rm W}^{-}|$. It is noted that the increment of $\Delta V_{\rm O}^{1}$ increases steeply around $|V_{\rm W}^{-}|$ between 2 and 2.5 V. This means that,

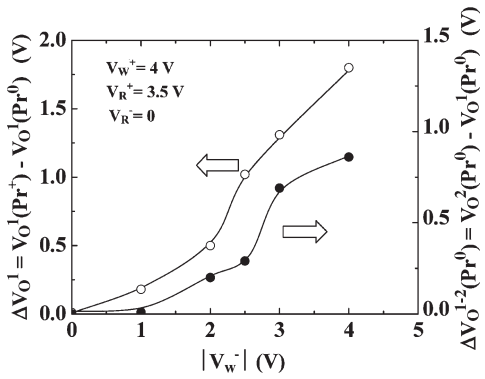

Fig. 6. $|V_{\rm W}^{-}|$ dependences of $\Delta V_{\rm O}^{1}=V_{\rm O}^{1}(P_{\rm r}^{+})-V_{\rm O}^{1}(P_{\rm r}^{0})$ and $\Delta V_{\rm O}^{1-2}(P_{\rm r}^{0})=V_{\rm O}^{2}(P_{\rm r}^{0})-V_{\rm O}^{1}(P_{\rm r}^{0})$. $\Delta V_{\rm O}^{1}$ is the difference in $V_{\rm O}$ between the $P_{\rm r}^{+}$ and $P_{\rm r}^{0}$ states at the first reading, and $\Delta V_{\rm O}^{1-2}(P_{\rm r}^{0})$ is the difference in $V_{\rm O}$ of the $P_{\rm r}^{0}$ state between the first and the second reading time. In this case, the previous reading pulse with $V_{\rm R}^{-}=0$ was used.

in this range, the polarity of the remanent polarization of the $P_{\rm r}^{0}$ state is probably changed from positive to negative and that the fraction of the domain switching from downward to upward per unit of $|V_{\rm W}^{-}|$ is the largest. We can also see from this figure that $\Delta V_{\rm O}^{1-2}(P_{\rm r}^{0})$ increases gradually with $|V_{\rm W}^{-}|$ up to 2.5 V and then abruptly increases from $|V_{\rm W}^{-}|=2.5$ to 3 V. This abrupt increase indicates that the nonreturning domains are significantly generated in the range of 2.5–3 V. Therefore, from the result of Fig. 6, it can be said that the appropriate $|V_{\rm W}^{-}|$ is located near 2.5 V. The next step to seek for more appropriate $V_{\rm W}^{-}$ was performed simultaneously with $V_{\rm R}^{-}$.

Fig. 7(a) shows the typical dependences of the output voltages $V_{\rm O}(P_{\rm r}^{+})$ and $V_{\rm O}(P_{\rm r}^{0})$ for the $P_{\rm r}^{+}$ and $P_{\rm r}^{0}$ states, respectively, on the number of reading times for different values of $V_{\rm R}^{-}$, where $V_{\rm R}^{-}=0$, -1, -1.8, -2.1, and -3 V. For the $P_{\rm r}^{0}$ state, $V_{\rm W}^{+}=4$ V and $V_{\rm W}^{-}=-2.6$ V were used. It can be seen from this figure that $V_{\rm O}(P_{\rm r}^{+})$ at $V_{\rm R}^{-}\geq -2.1$ V is constant and does not vary with the number of reading times. However, at $V_{\rm R}^{-}=-3$ V, it decreases gradually with the reading time, which means that increasing $|V_{\rm R}^{-}|$ over 2.1 V induces a nonreturning domain even in the $P_{\rm r}^{+}$ state and degrades the memory state. On the other hand, although $V_{\rm O}(P_{\rm r}^{0})$ increases with the reading time at $V_{\rm R}^{-}\geq -1.8$ V, the increment decreases with $|V_{\rm R}^{-}|$. This is because the volume of the nonreturning domain is reduced with increasing $|V_{\rm R}^{-}|$. Moreover, at $V_{\rm R}^{-}=-2.1$ and -3 V, $V_{\rm O}(P_{\rm r}^{0})$ is kept constant and does not change for any number of reading times, which means that the generation of the nonreturning domain is completely suppressed for the $P_{\rm r}^{0}$ state. From this result, at $|V_{\rm R}^{-}|=2.1$ V, the difference between $V_{\rm O}^{n}(P_{\rm r}^{+})$ and $V_{\rm O}^{n}(P_{\rm r}^{0})$, $\Delta V_{\rm O}^{n}$, remains constant, and both memory states are stable to the ten reading times. Otherwise, $\Delta V_{\rm O}^{n}$ decreases due to reading out, which is unfavorable for data decoding as memory device. The saturation of $V_{\rm O}^{n}(P_{\rm r}^{+})$ and $V_{\rm O}^{n}(P_{\rm r}^{0})$ with the reading time means that the new memory states are rebuilt from the initial memory states by applying reading pulse consecutively. These new states result from balance in volume of the domain switched between upward and downward due to the application of the combined reading pulse.

Fig. 7(b) shows the dependences of $\Delta V_{\rm O}^{10}=V_{\rm O}^{10}(P_{\rm r}^{+})-V_{\rm O}^{10}(P_{\rm r}^{0})$, the difference in $V_{\rm O}$ between the $P_{\rm r}^{+}$ and $P_{\rm r}^{0}$ states

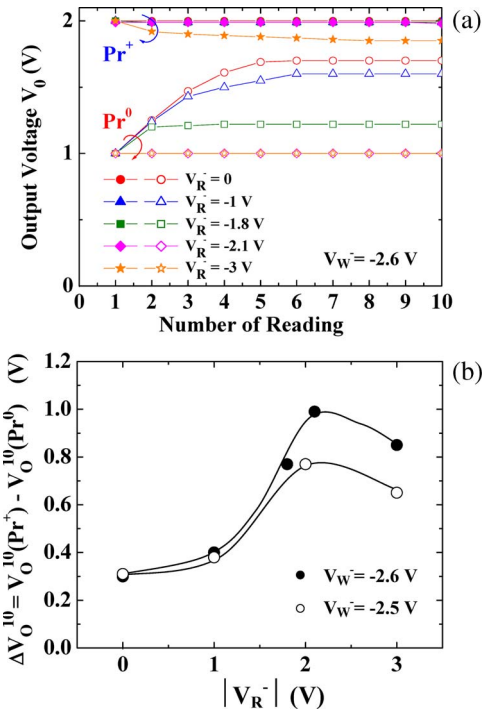

Fig. 7. (a) Characteristics of output voltage $V_{\rm O}$ for the $P_{\rm r}^{+}$ and $P_{\rm r}^{0}$ states versus the number of readings for different values of $V_{\rm R}^{-}$ with $V_{\rm W}^{-} = -2.6$ V, and (b) $|V_{\rm R}^{-}|$ dependences of $\Delta V_{\rm O}^{10} = V_{\rm O}^{10}(P_{\rm r}^{+}) - V_{\rm O}^{10}(P_{\rm r}^{0})$ for $V_{\rm W}^{-} = -2.5$ and -2.6 V. $\Delta V_{\rm O}^{10}$ is the difference in $V_{\rm O}$ between the $P_{\rm r}^{+}$ and $P_{\rm r}^{0}$ states at the tenth reading. In this case, $V_{\rm W}^{+} = 4$ V and $V_{\rm R}^{+} = 3.5$ V.

at the tenth reading, on $V_{\rm R}^{-}$ for $V_{\rm W}^{-} = -2.5$ and -2.6 V. From these characteristics, we can find better values of $V_{\rm W}^{-}$ and $V_{\rm R}^{-}$ from a viewpoint of distinct memory operation. Around $|V_{\rm R}^{-}| = 2.1$ V, $\Delta V_{\rm O}^{10}$ for both V_{W}^{-} values reach the maximum values because of almost-perfect suppression of the nonreturning domain for their memory states, as mentioned earlier. Also, because $\Delta V_{\rm O}^{10}$ for $V_{\rm W}^{-} = -2.6$ V is larger than that for $V_{\rm W}^{-} = -2.5$ V, the former value of $V_{\rm W}^{-}$ is more desirable.

By investigating the pulse heights as mentioned previously, as appropriate operation parameters, we determined $V_{\rm W}^{+} = 4$ V and $V_{\rm W}^{-} = -2.6$ V for the $P_{\rm r}^{0}$ state, and $V_{\rm R}^{+} = 3.5$ V and $V_{\rm R}^{-} = -2.1$ V for the combined reading pulse. The voltage ranges for the writing and reading pulses seem narrow if the memory array requires the largest $\Delta V_{\rm O}$ under nondestructive readout. However, if $\Delta V_{\rm O}$ is not required to be the largest but large enough for the sense signal, their ranges are probably not so narrow in practice. The operation voltages, e.g., $V_{\rm W}^{-}$ and $V_{\rm R}^{-}$, strongly depend on not only memory structure such as ferroelectric thickness, $C_{\rm i}$, transconductance of the reading transistor, and so on, but also ferroelectric properties such as $C_{\rm fh}$, $C_{\rm fl}$, $E_{\rm c}$, curvature of $P{-}V$ loop, and so on. Therefore, the range of operation voltage can be extended so that the memory array of IF-FET is commercialized, provided that the memory structure and ferroelectric properties of $C_{\rm f}$ are improved properly.

B. Read-Out Characteristics

Fig. 8 shows the comparison of reading endurance characteristics between (a) the previous operation method and (b) the improved method in this paper, where, in the previous method, $V_{\rm W} = 4$ V for the $P_{\rm r}^{+}$ state, $V_{\rm W} = -4$ V for the $P_{\rm r}^{-}$ state, and $V_{\rm R} = 3.5$ V. We can see from Fig. 8(a) that, although $V_{\rm O}(P_{\rm r}^{+})$ is constant, $V_{\rm O}(P_{\rm r}^{-})$ quickly increases with the reading cycle because the $P_{\rm r}^{-}$ state is degraded due to the generation of nonreturning domains. As a result, above 10^{4} reading cycles, $\Delta V_{\rm O} = V_{\rm O}(P_{\rm r}^{+}) - V_{\rm O}(P_{\rm r}^{0})$ is reduced to small value of less than 0.11 V, which is too small to distinguish both memory states. Therefore, we can say that the reading endurance of the previous operation is very poor. However, by using our improved operation method, the reading endurance is extended significantly to over 10^{8} reading cycles, as shown in Fig. 8(b), because the $P_{\rm r}^{0}$ state can be recovered after each reading cycle. Although the output voltage $V_{\rm O}(P_{\rm r}^{+})$ remains even above 10^{8} reading cycles, $V_{\rm O}(P_{\rm r}^{0})$ increases slightly. One possible reason for this is quality degradation of the PZT film due to a number of reading cycles. For example, if the $P{-}E$ hysteresis loop is shifted toward the negative voltage side, the $P_{\rm r}^{0}$ memory state approaches the $P_{\rm r}^{+}$ state, and $V_{O}(P_{\rm r}^{0})$ increases. In order to prevent this phenomenon, the quality of the ferroelectric film should be more stabilized. From this result, it can be concluded that our improved operation method is very effective for the reading endurance. Using a high-quality ferroelectric film like a commercial film, the intrinsic reading endurance is expected to be $10^{12}{-}10^{13}$ cycles, which is the reported value for FeRAM in general. We reported in our previous papers that the reading endurance is about 10^{6} cycles for the $P_{\rm r}^{-}$ state, but the result of Fig. 8(a) shows a much smaller number of cycles of the endurance than this [21], [22]. The MOSFET used previously was not commercial, but was home-made, and it was connected with the diodes to simulate a writing transistor. Although the commercial MOSFET used in this paper is not connected with either a writing transistor or diodes, it has a protection circuit composed of diodes connected between the source and the gate and between the drain and the gate. The leakage current of the protection circuit is much larger than that of the simulation diodes by about two orders of magnitude. The leakage current which supplies some negative charge on the intermediate electrode degrades the $P_{\rm r}^{-}$ state at each reading operation. Therefore, the $P_{\rm r}^{-}$ state in this study was destroyed more quickly than the previous one. Taking this into account, we can also say that the improved operation method overcomes drawbacks due to an inevitable small leakage current through the MOSFET gate.

Even in the previous memory states of $P_{\rm r}^{+}$ and $P_{\rm r}^{-}$, it seems that nearly nondestructive readout is possible without using a $P_{\rm r}^{0}$ state if $V_{\rm R}^{+}$ and $V_{\rm R}^{-}$ pulses with the optimized heights are used. In order to return the read-out $P_{\rm r}^{-}$ state to the initial state almost without the nonreturning domain, we need such a high $|V_{\rm R}^{-}|$ that the $P_{\rm r}^{+}$ state may change negative and be destroyed. It was found that $V_{\rm R}^{-}$ brought the $P_{\rm r}^{+}$ state close to the $P_{\rm r}^{-}$ one to suppress the nonreturning domain in the $P_{\rm r}^{-}$ state, which is a destructive readout. Therefore, it can be concluded that a nondestructive readout is impossible without using a $P_{\rm r}^{0}$ state. Also, using a $P_{\rm r}^{0}$ state is more favorable with respect to low-power consumption, because $|V_{\rm R}^{-}|$ for $P_{\rm r}^{0}$ is lower.

Fig. 9 shows the retention characteristics of the $P_{\rm r}^{+}$ and $P_{\rm r}^{0}$ states for the improved operation method. After each data

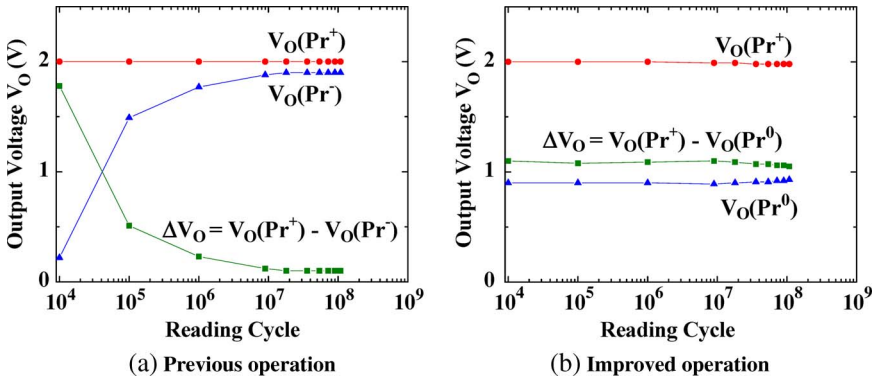

Fig. 8. Reading endurance characteristics of (a) the previous operation method and (b) the improved operation method. In (a), $V_W = 4$ V for the P_r^+ state, $V_W = -4$ V for the P_r^- state, and $V_R = 3.5$ V for the reading out. In (b), $V_W = 4$ V for the P_r^+ state, $V_W^+ = 4$ V and $V_W^- = -2.6$ V for the P_r^0 state, and $V_R^+ = 3.5$ V and $V_R^- = -2.1$ V for the reading out.

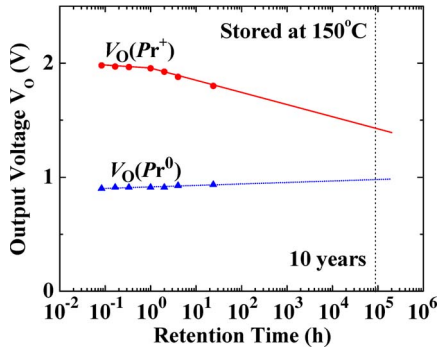

Fig. 9. Retention characteristics for the improved operation method. $V_W = 4$ V for the P_r^+ state, $V_W^+ = 4$ V and $V_W^- = -2.6$ V for the P_r^0 state, and $V_R^+ = 3.5$ V and $V_R^- = -2.1$ V for the reading out.

writing, the two memory states were stored at 150 °C in air for various retention times up to 24 h. We can see from this figure that $V_O(P_r^+)$ decreases more quickly than $V_O(P_r^0)$ increases with the retention time. Since the P_r^+ state has a much higher energy of electric static potential than the ground state, it is gradually depolarized by thermal energy. In contrast with the P_r^+ state, the P_r^0 state is much stabler in energy because it is little polarized, which can lead to a stable output signal for a long retention time. As a possible reason for the slight increase in $V_O(P_r^0)$ with the retention time, it can be considered that the initial P_r^0 state is not perfectly nonpolarized and that the ferroelectric property is slightly changed due to the storage at 150 °C. Extrapolating the fitting lines along the data for the P_r^+ and P_r^0 states individually, as shown in Fig. 9, we can estimate that $\Delta V_O = V_O(P_r^+) - V_O(P_r^0)$ will be larger than 0.4 V even after a ten-year storage at 150 °C. As $\Delta V_O = 0.4$ V is a sufficient signal to distinguish the memory state, it can be said that IF-FET memory has good retention characteristics. This results not only from the nondepolarization field in the ferroelectric film during retention like FeRAM but also from using the energetically stabler P_r^0 state with almost nonpolarization. Therefore, IF-FET memory can solve the serious problem of short retention time which prevails in the conventional F-FET memory.

In an actual memory array, writing and reading disturbances should be avoided. In the case of IF-FET, since combined reading pulse serves nondestructive readout, reading disturbance can be negligible. However, the writing disturbance, in particular, of the P_r^0 state due to P_r^+ writing is serious. Because P_r^+-writing pulse is always positive, the nonpolarized state of P_r^0 may change to positive and approach the P_r^+ state with repeating P_r^+ writing. If the nonselected memory cell is electrically floated perfectly or the plate line of the nonselected cell is biased positively corresponding to the P_r^+-writing pulse, the writing disturbance of the P_r^0 state might be free. However, these compensation operations for disturbance free are complicated and difficult technically. In order to suppress P_r^0 disturbance due to P_r^+ writing practically, we should investigate in the future.

V. Conclusion

We investigated the reading and writing of IF-FET in order to achieve perfect nondestructive readouts. In the previous operation method, although the difference in output voltage ΔV_O between the P_r^+ and P_r^- states is sufficient at the first reading time, the nondestructive readout for the P_r^- state is seriously degraded because of large amounts of remaining charge Q_r on C_i due to the nonreturning domains generated after reading out. In order to reduce Q_r, the P_r^0 state was used as a new memory state instead of the P_r^- state. The P_r^0 state was induced by applying a pulse combined with a positive voltage V_W^+ and a negative voltage V_W^-. V_W^+ was to reset the previously written memory states, and V_W^- was to control the amount of remanent polarization. When the negative remanent polarization is smaller, Q_r is also smaller. However, ΔV_O measured by reading out is too small to decode the memory state. In order to both maintain a large ΔV_O and suppress Q_r sufficiently, for data reading, a negative voltage V_R^- was applied following a positive voltage V_R^+ which was determined for distinct decoding. By increasing $|V_R^-|$, the downward domains switched by V_R^+ can be returned to the initial upward domains, and the P_r^0 state can be recovered after each reading. However, excessive $|V_R^-|$ destroys the P_r^+ state. Therefore, we investigated in detail the heights of V_W^- and V_R^- from the viewpoint of zero Q_r and large ΔV_O. Under appropriate conditions, where $V_W^+ = 4$ V, $V_W^- = -2.6$ V, $V_R^+ = 3.5$ V, and $V_R^- = -2.1$ V, nondestructive readout was achieved. By using the improved operation method,

it was verified experimentally that the reading endurance can reach more than 10^8 cycles. This result indicates that the intrinsic endurance of IF-FET is expected to be more than 10^{12} cycles, which is comparable with that of FeRAM. Furthermore, it was shown that the retention time of IF-FET at 150 °C can exceed about ten years. From these results, we can conclude that IF-FET memory array can be a very promising candidate for future memories if the writing disturbance is sufficiently prevented.

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