Organic field effect transistors with dipole-polarized polymer gate dielectrics for control of threshold voltage

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The authors demonstrate organic field effect transistors (OFETs) with a dipole-polarized polyurea for the gate dielectrics. In the dielectrics, the internal electric field induces the mobile charge carrier in the semiconductor layer to the semiconductor-dielectric interface. OFETs with dipole-polarized gate dielectrics exhibit lower threshold voltage. With nonpolarized gate dielectrics, the threshold voltage was −11.4 V, whereas that decreased to −5.3 V with polarized gate dielectrics. In addition to the threshold voltage, polarized gate dielectrics reduced subthreshold swing from 4.1 to 2.4 V/decade at the gate voltage of −20 V. These results show that dipole-polarized polyurea gate dielectrics allow us to operate OFETs with lower power consumption. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2783180]

In recent years organic field effect transistors (OFETs) have received increased attention due to their unique advantages, which include a variety of molecular designs, light weight, low cost of fabrication, and mechanical flexibility.[1] Although much effort has gone into developing OFETs having organic materials for the gate dielectric layer, there are several issues to be solved. One is the high operating voltage, which often exceeds 20 V. The reduction of threshold voltage and the subthreshold slope leads to low-voltage operation. For the low-voltage operation, the material development for the gate dielectrics is one of the key issues since the choice of the gate dielectrics largely affects to the electric properties of OFETs.[2]

Several approaches have been proposed to control threshold voltage and the subthreshold slope with gate dielectrics. Introducing high dielectric constant (high-*k*) material to gate dielectrics would induce greater charge in the semiconductor layer at a given gate voltage so that the device can be operated at a lower voltage.[3–6] Use of inorganic oxides as the high-*k* material may have some drawbacks such as incompatibility with plastic substrate due to the high process temperature and difficulty of patterning. For further development of flexible electronics, low-voltage OFETs totally composed of organic materials would be an ideal system. Several strategies for the improvement of operational voltage using organic dielectrics have been reported. For example, polymer gate dielectrics were mixed with metal oxide nanoparticles to increase in dielectric constant.[7,8] However, the surface of dielectric would become rougher and the large leakage current was observed with increasing content of the nanoparticles. In another approach, self-assembled monolayers (SAMs) were employed as a gate dielectrics.[9] Although ultrathin monolayer less than 10 nm would be effective for reducing operation voltage, it would be a big technical challenge for making pin-hole free monolayer film in large area. Thus, alternative approaches for organic dielectrics are desired for low-voltage OFETs where the dielectrics should be compatible with flexible large-area substrate and low-cost production process.

The effect of electric dipoles on the electronic characteristics of OFETs has been reported.[10,11] On SiO_2 gate dielectrics, SAMs were applied by solution process. The control of threshold voltage in OFETs was demonstrated by changing dipole moment of SAM on SiO_2. The results indicate that aligned dipoles of SAMs on SiO_2 change surface potential of gate dielectrics and induce mobile charge carriers in the active layer. Although these techniques were effective on OFET electronic characteristics, OFETs totally composed of organic materials would be an ideal system for further development of flexible electronics.

Here, we report an OFET with dipole-polarized polymer gate dielectrics. These dipole-polarized polymer gate dielectrics enabled one to operate the OFETs with significantly lower operating voltages, less than 6 V. Dipole-polarized polymer films show electric characteristics such as piezoelectricity and pyroelectricity. The properties of dipole-polarized polymer films have been extensively investigated. Polyurea is one of the polymers whose characteristics have been reported.[12,13] However, these films have not been applied to any application for gate dielectrics in OFETs despite their good insulation characteristics.

If the dipoles of polyurea are uniformly oriented in one direction, the internal electric field is formed. This electric field induces the mobile charge carrier in the semiconductor layer to the semiconductor-dielectric interface. As a result, the operation voltage shifts to lower voltage. The internal electric field acts as offset of gate voltage and the strength of the field increases as the film thickness increases. In addition, increasing thickness of gate dielectric would reduce the leak-

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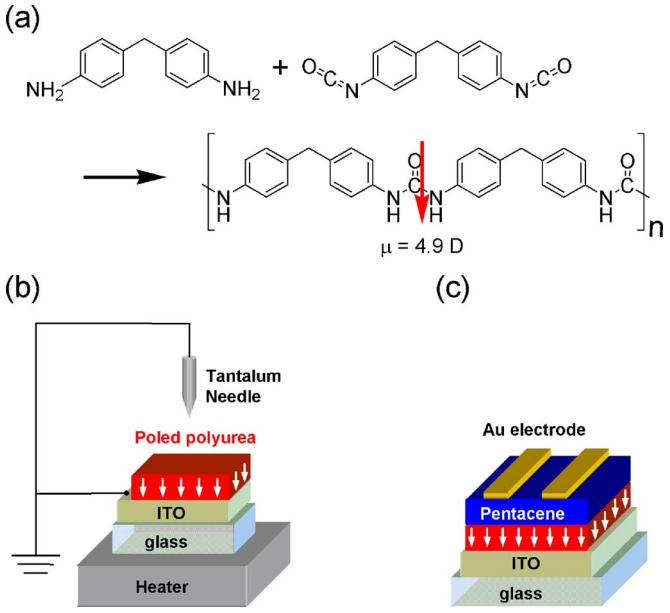

FIG. 1. (Color online) Preparation scheme of OFETs with polarized gate dielectrics. (a) Reaction scheme of polyurea by vapor deposition polymerization. The dipole moment of a urea group is 4.9 D (Refs. 10 and 11). Schematic representations of corona poling process of (b) polyurea gate dielectrics and (c) OFETs with polarized gate dielectrics.

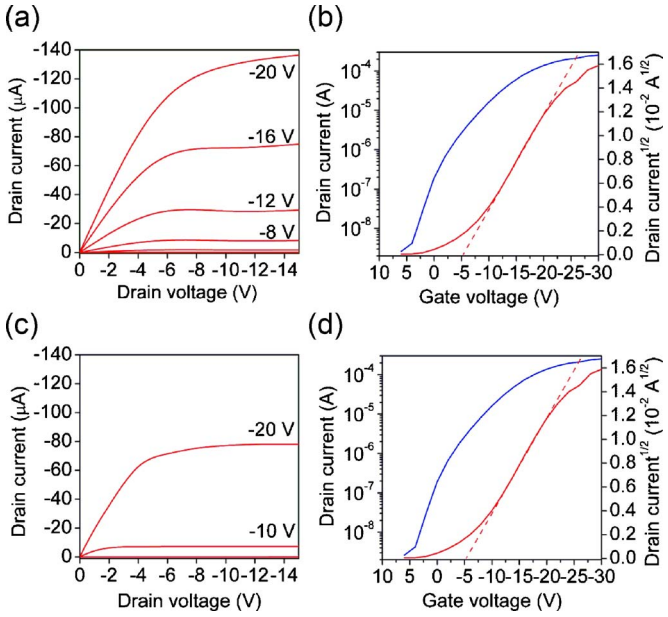

FIG. 2. (Color online) Device characteristics of devices 1 and 2. (a) and (b) show the output characteristics and transfer characteristics of devices 1. (c) and (d) show the output characteristics and transfer characteristics of devices 2. The channel width and channel length are 24 500 and 75 μm.

age current through the gate dielectrics with preventing increase in gate voltage.

The preparation procedure of OFETs is shown in Fig. 1. Indium tin oxide on glass was used as the gate electrode, which was cleaned by ultrasonication in acetone, de-ionized water, and isopropyl alcohol. The polyurea layer was deposited by the vapor deposition polymerization method.[14] The monomers used to synthesize the polyurea were 4,4-diaminodiphenyl methane and 4,4-diphenyl methane diisocyanate. Polarization of the polyurea film was performed by corona poling. Application of a high direct current electric field to the polyurea film at 200 °C oriented the permanent dipole of the urea segment parallel to the electric field [Fig. 1(b)]. During the corona poling, high voltages of +6 kV were applied to a tantalum needle at a distance of 5 cm from the film surface. This polarization was fixed by further polymerization reaction during the poling process.[15] To apply these films to OFETs with top-contact geometry, thin films of pentacene (Aldrich, purified by vacuum sublimation) were formed by vacuum deposition at the rate of 0.05 nm s^{-1} on polarized dielectrics (denoted as device 1) and nonpolarized dielectrics (device 2), followed by the deposition of a gold top electrode at the rate of 0.05 nm s^{-1}. The film thickness of both pentacene and gold was 50 nm. The channel length (W) and width (L) is 75 and 24 500 μm, respectively. Electric characteristics of OFETs were measured with a Keithley 4200 semiconductor characterization system in an ambient atmosphere.

Figure 1(c) shows the schematic representation of the OFETs with polarized dielectrics. Dipoles uniformly oriented in one direction cause the electric field, which induces the mobile charge carrier in the semiconductor (pentacene) layer at the semiconductor-dielectric interface.

Figure 2 shows the output characteristics for device 1 [Fig. 2(a)] and device 2 [Fig. 2(b)]. These device characteristics are consistent with the behavior of a p-type semiconductor. The I_D value of device 1 at V_G=−20 V is 1.8 times larger than that of device 2 that indicates the mobile charge carrier in the semiconductor layer is induced by polarized gate dielectrics. Considering that the thicknesses of the gate dielectric layers were exactly the same (420 nm), it is clear that polarized gate dielectrics enhance the I_D value at any given gate voltage.

In the saturation regime, the carrier mobility was estimated by fitting the plot of the square root of I_D vs V_G with the following equation:[16]

$$I_D = \frac{WC\mu}{2L}(V_G - V_T)^2, \tag{1}$$

where C is the capacitance per unit area of the gate dielectrics, μ is the carrier mobility, and V_T is the threshold voltage. We have measured the capacitance of polarized gate dielectric and the value was 10.6 nF cm^{-2} at 100 kHz. Figures 2(b) and 2(d) show the transfer characteristics of devices 1 and 2. For device 1, V_T, the subthreshold swing, and the on/off current ratio were −5.3 V, 2.4 V/decade, and 9.7×10^4 at V_D=−20 V, respectively. The mobility of device 1 was calculated to be 0.042 $cm^2\ V^{-1}\ s^{-1}$. In contrast, device 2 exhibited that the V_T, the subthreshold swing, and the on/off current ratio were −11.4 V, 4.1 V/decade, and 5.2×10^4 at V_D=−20 V, respectively. The mobility of device 2 was 0.070 $cm^2\ V^{-1}\ s^{-1}$, which is slightly larger than that of device 1. By using polarized dielectrics, device 1 demonstrated significantly lower threshold voltage more than 6 V. The polarized gate dielectrics have an internal electric field due to the alignment of permanent dipoles so that the charge carrier in the semiconductor layer is induced to the semiconductor-dielectric interface without external electric field. Indeed, as shown in Fig. 2(b), p-type conductive channel exists at zero gate bias (V_G=0 V) in device 1 whereas the normally off type characteristic was observed in device 2.

By reference to Eq. (1), there are three possible origins of increase in the drain current of the device with polarized gate dielectric. Those are the increases in the dielectric con-

stant and carrier mobility or the decrease in the threshold voltage. First, the dielectric constant $k=4.1$ was calculated using the measured capacitance of $10.6\ \mathrm{nF\,cm^{-2}}$ and the thickness of gate dielectric. This value is close to or slightly smaller than the reported value $k=4.4$ of unpolarized gate dielectric.[15] This result suggests that the polarization of gate dielectric does not increase the dielectric constant. Second, the carrier mobility of the device with polarized dielectric was decreased compared with that of the device with nonpolarized film. Thus the increase in the I_D was ascribed to the shift of V_T by the internal electric field owing to the polarized dielectric.

To obtain more insights of the shift of V_T, we estimate the contribution of the internal electric field of the polarized gate dielectric. To make this point clear, V_T was expressed as $V_T=V_{T0}+V_{\mathrm{int}}$, where V_{T0} is the threshold voltage without the effect of the polarized dielectrics and V_{int} is the voltage attributed to the internal electric field of the polarized dielectrics. The internal electric field E was calculated by dividing the V_{int} by the film thickness d. The observed shift of threshold voltage between devices 1 and 2 was 6.1 V and the thickness of dielectrics was 420 nm, and then E was calculated to 1.5×10^7 V/m. The theoretical value induced by assembling dipole moment in dielectrics is given by

$$E=\frac{V_{\mathrm{int}}}{d}-\frac{p}{\varepsilon_0}=-\frac{\mu}{v\varepsilon_0}, \tag{2}$$

where p is the constant polarization density, ε_0 is the vacuum permittivity, μ is the dipole moment of urea group, and ν is the volume per molecule. The value of ν is calculated to be $0.37\ \mathrm{nm^3}$. When dipoles are perfectly aligned, the theoretical value of E is calculated to be 4.8×10^9 V/m. This value is much larger than the observed value and the ratio of oriented urea group is estimated to be $\sim0.25\%$ of total amount of urea group. Further optimization of poling condition would align more dipoles in dielectrics and as a result large shift of V_T can be obtained.

The subthreshold swing of device 1 was lower than that of device 2. When we operate the devices, application of gate voltage would induce additional orientation of dipoles in the dielectrics of devices 1 and 2. Since the dielectrics of device 1 have been subject to poling process, some dipoles are already aligned. The prealigned dipoles may induce additional internal electric field which would cause the difference of drain current with applying gate voltage. Thus the subthreshold swing of the device 1 was better than device 2.

The carrier mobilities of the devices measured in this study, 0.044 for polarized gate dielectrics and 0.077 for unpolarized gate dielectrics, were about one order of magnitude smaller than the reported values of the devices using other polymer gate dielectrics.[2] Also we noticed that the carrier mobility of device 1 was about half of that of device 2. The reduction in mobility with increasing dielectric constant of gate dielectrics has been reported.[17] In that context, the larger Coulomb interaction between charge carriers and induced dipoles of gate dielectrics causes the reduction of the mobility.[18] In our devices, aligned permanent dipoles of urea group may interact with charge carriers at the interface between pentacene and polyurea gate dielectrics. As a result, the carrier mobility may be decreased. For improving carrier mobility, it may be necessary to reduce interaction between surface dipoles and charge carriers. Based on the hypothesis, another polymer buffer layer, PMMA, was inserted between the pentacene layer and the polyurea gate dielectrics. Indeed, the devices with double gate dielectrics showed enhanced mobility such as $0.19\ \mathrm{cm^2\,V^{-1}\,s^{-1}}$ (polarized polyurea/PMMA) and $0.13\ \mathrm{cm^2\,V^{-1}\,s^{-1}}$ (unpolarized polyurea/PMMA). The details of the devices with double gate dielectrics will be reported elsewhere.

In conclusion, we have demonstrated an organic transistor with polarized gate dielectrics based on poled polyurea. The threshold voltages of the OFETs become significantly lower. We believe that these gate dielectrics may open for the route to mass production of low-voltage flexible OFETs.

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