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Description	

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Generation of Power-Constrained Scan Tests and Its Difficulty

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Abstract

This paper proposes a test generation framework to generate stuck-at tests for a scan circuit under both peak shift and capture power limits. A concept of "complete fault efficiency under a power budget" is introduced, and it is pointed out that existing test-generation-based techniques for test power lack this completeness. Some analytical data obtained by using the proposed framework are presented to show the difficulty of generating test patterns that meet given limits for shift-in, shift-out and capture power, simultaneously. To relax the difficulty, this paper also describes a heuristic procedure using a cone analysis that definitely derives scan tests with low shift-in power and that reduces the search space during test generation. From the point of view discussed in this paper, further work should be undertaken in the future.

Keywords: scan circuit, peak power, power-constrained test generation, complete fault efficiency under a power budget, cone analysis

1 Introduction

Excessive power dissipation during scan testing is one of the main concerns for today's complex digital circuits. This is because such excessive power dissipation affects the reliability and manufacturing yield of circuits. The peak power and average power, therefore, have to be controlled in manufacturing test. To handle this problem, many approaches have been proposed in [1, 2] which can be classified into two categories: scan-architecture-based and test-generation-based (TG-based) ones. In a method based on the former strategy, a scan circuit is modified to reduce test power by using some techniques such as scan cell modification, scan chain re-ordering and clock-gating. Obviously, this kind of strategies requires additional hardware elements which can impact on the original design. Any TG-based methods, on the other hand, never impact on the original design. This property is definitely preferable to a scan-architecture-based method.

Here, we briefly review existing TG-based methods for low power test. In this paper, we focus on peak power during scan testing because it is independent of the test frequency and hence is much difficult to control compared to controlling average power [3]. Most of existing TG-based methods for low power test, such as [3, 4, 5, 6], basically use X-filling techniques where an unspecified bit of a test pattern is filled with '0' or '1' on the basis of some criteria after test generation or during test generation. If the peak power during testing a scan circuit exceeds a given power budget, its test results can be invalidated due to a power violation. Since this violation can occur during any of shift-in, shift-out and capture cycles, one should take into account all of them in generating test patterns. Some of existing TG-based methods lack this requirement. More importantly, any existing TG-based methods can never provide a complete solution to whether a fault is testable under a given power budget. This paper provides a complete solution to this problem.

In this paper, we propose a power-constrained test generation model for stuck-at faults to control the peak power during both of the scan shift and capture cycles, simultaneously. Given a power budget for a scan circuit, power limiters for shift-in, shift-out and capture power are synthesized. Then, those limiters are attached to the combinational part of a scan circuit to construct a power-constrained test generation model. By using this obtained model, one can generate test patterns that meet the power limits, and can completely identify untestable faults under the limits. In this paper, we point out that it is hard to generate test pat-

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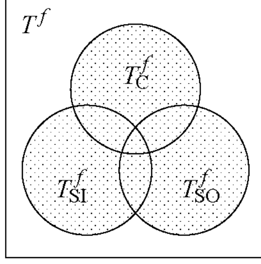

Figure 1: Inclusion relation among test sets for a fault under a power budget

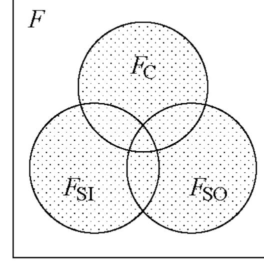

Figure 2: Inclusion relation among detectable faults under a power budget

terns that meet a given power budget even for a small circuit. To alleviate this problem, we also present a heuristic procedure using a cone analysis that definitely derives scan tests with low shift-in power and that reduces the search space during test generation.

2 Preliminaries

2.1 Power Estimation

In this paper, we target stuck-at faults in a full-scan circuit with a single scan chain, and assume that its chain order is fixed. To estimate the power consumed by a test pattern t, we adopt the weighted transition and capture transition metrics in [2]:

$$WT_{\mathrm{SI}}(t) = \sum_{i=1}^{n-1} (FF_i(t) \oplus FF_{i+1}(t)) \cdot i$$

for shift-in power;

$$WT_{\mathrm{SO}}(t) = \sum_{i=1}^{n-1} (FF_i^+(t) \oplus FF_{i+1}^+(t))(n-i)$$

for shift-out power; and

$$CT(t) = \sum_{i=1}^{n} (FF_i(t) \oplus FF_i^+(t))$$

for capture power. In the above metrics, n is the number of scan flip-flops (FFs), $FF_i(t)$ denotes the value stored in the i-th scan FF before applying t to the circuit, and $FF_i^+(t)$ is its stored response. Note that the scan FF connected to the external scan input is on the first position of the chain.

2.2 Problems of Existing Methods

Figure 1 shows the inclusion relation among test sets for a fault f under a power budget $P = (L_{\mathrm{SI}}, L_{\mathrm{SO}}, L_{\mathrm{C}})$ where L_{SI}, L_{SO} and L_{C} correspond to peak power limits for shift-in, shift-out and capture cycles, respectively. In Fig. 1, T^f is the set of all the possible test patterns for f in a situation where a given power budget is unlimited, i.e., $P = (\infty, \infty, \infty)$. For a power budget of $(L_{\mathrm{SI}}, \infty, \infty)$, T^f_{SI} $(\subset T)$ denotes the set of all the possible test patterns for f that meet the power budget. Test sets T^f_{SO} and T^f_{C} are defined similarly. Figure 2 shows the inclusion relation among detectable faults under P. In Fig. 2, F is the set of all the detectable faults under $P = (\infty, \infty, \infty)$. For a power budget of $(L_{\mathrm{SI}}, \infty, \infty)$, F_{SI} $(\subset F)$ denotes the set of all the detectable faults under the power budget. Fault sets F_{SO} and F_{C} are defined similarly. If a fault f $(\in F)$ does not belong to $F_{\mathrm{SI}} \cap F_{\mathrm{SO}} \cap F_{\mathrm{C}}$, f is untestable under P, i.e., $T^f_{\mathrm{SI}} \cap T^f_{\mathrm{SO}} \cap T^f_{\mathrm{C}} = \emptyset$. On the basis of this new untestable class of faults, a concept of "complete fault efficiency under a power budget" can naturally be introduced. One goal of power-constrained test generation is to achieve complete fault efficiency under a power budget.

Now, by using the above notations, let us clarify the problems of existing TG-based methods, such as [3, 4, 5, 6], stated in the previous section. The methods in [5, 6] attempt to minimize peak power by X-filling techniques. Thereby, one can obtain low peak power test patterns. However, as long as these methods are used, nobody knows whether a fault f $(\in F)$ belongs to $F_{\mathrm{SI}} \cap F_{\mathrm{SO}} \cap F_{\mathrm{C}}$ under a power budget P, because the methods do not consider P. The method in [3], on the other hand, considers a power budget in its procedure where X-filling and pattern ordering techniques are used. Indeed, although one can obtain test patterns that meet the power budget, this method lacks completeness because of assuming a pre-generated test set. Clearly, it is never guaranteed that the test cubes for a fault f $(\in F)$ in the pre-generated test set belong to $T^f_{\mathrm{SI}} \cap T^f_{\mathrm{SO}} \cap T^f_{\mathrm{C}}$ under P. This implies that some detectable faults in $F_{\mathrm{SI}} \cap F_{\mathrm{SO}} \cap F_{\mathrm{C}}$ under P can escape during scan testing. In [4], a limit of peak capture power is successfully handled during test generation,

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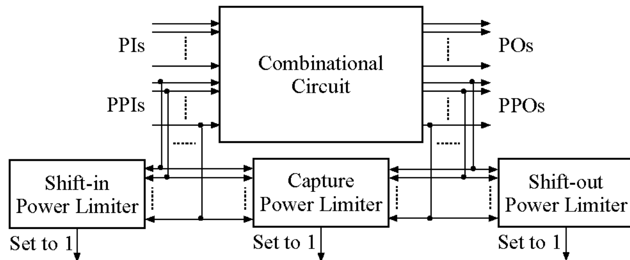

Figure 3: Power-constrained test generation model for a scan circuit

and therefore, test patterns that meet the limit can be generated. Unfortunately, this method never guarantees completeness because of adopting some heuristic decisions that lose completeness during test generation. Furthermore, this method does not consider peak shift power. As described above, there have been no existing TG-based methods that guarantee completeness so far.

3 Power-Constrained Test Generation

3.1 Power-Constrained Test Generation Model

Before we describe our proposed model for power-constrained test generation, we now introduce our previous work in [7] which provides a test generation scheme using checker circuits. The test generation scheme in [7] can add new features to existing test generation tools without modifying themselves. A checker circuit expresses some properties which should be satisfied during test generation, and the checker circuit is attached to the circuit under test to force a test generation tool to meet the properties. In [7, 8], the above scheme was used to handle path delay faults by using a stuck-at test generation tool. A possibility of handling scan test power was also suggested in [7, 8]. Recently, a method based on a similar scheme to our previous work has been proposed to generate power-aware test patterns for scan-based circuits [9]. The method in [9] can derive low shift power tests that meet a given power budget by using an off-the-shelf commercial test generation tool.

On the basis of our previous work, we present here a test generation model to achieve complete fault efficiency under a power budget of shift-in, shift-out and capture cycles. Figure 3 shows our proposed test generation model. In Fig. 3, PIs (resp. POs) denote the primary inputs (resp. primary outputs) of a scan circuit. PPIs (resp. PPOs) correspond to the outputs (resp. inputs) of the scan FFs. The respective power limiters are synthesized according to a given power budget P measured by the weighted transition and capture transition metrics. Each limiter outputs the value of '1' only if a test pattern meets its corresponding power limit. Otherwise, the value of '0' is produced. Thus, by giving additional constraints for the outputs of the limiters to an existing test generation tool, one can obtain power-safe tests that belong to $T^f_{\mathrm{SI}} \cap T^f_{\mathrm{SO}} \cap T^f_{\mathrm{C}}$ for every fault f ($\in F_{\mathrm{SI}} \cap F_{\mathrm{SO}} \cap F_{\mathrm{C}}$) under P. Furthermore, this model can completely identify whether a fault is testable under P, i.e., whether a fault belongs to $F_{\mathrm{SI}} \cap F_{\mathrm{SO}} \cap F_{\mathrm{C}}$.

The overall test generation procedure using the proposed model is summarized as follows. Let C and $P = (L_{\mathrm{SI}}, L_{\mathrm{SO}}, L_{\mathrm{C}})$ be the combinational part of a scan circuit and its power budget, respectively. Let F be a set of target faults. Then, a power-safe test set T for F is obtained by the following steps.

1. Design power limiters according to P.
2. Connect C to the limiters as shown in Fig. 3.
3. Apply a test generation tool to the model obtained in the previous step under constraints where every output of the limiters has to be '1.'

3.2 Case Study

In this subsection, we show some experimental results where power-constrained test generation based on our proposed framework was performed from various aspects on one ISCAS '89 benchmark circuit (s1196). The following experiments were done on a Linux workstation (CPU: AMD Opteron Processor 256 3.0 GHz, Memory: 16 GB).

The first experiment using our framework was performed to examine the correlation between detectable faults and power budgets. For reference, test patterns for 3,220 stuck-at faults in s1196 were generated under the unlimited power budget, i.e., $P = (\infty, \infty, \infty)$ by using a commercial test generation tool. This result is listed in column "Unlimited" of each of Tables 1–3. In Tables 1–3, columns "#det," "#unt" and "#abt" denote the number of detected faults, identified untestable faults and aborted faults, respectively. Columns "#vec" and "TGT" denote the number of generated test patterns and test generation time, respectively. As shown in "Unlimited," the maximum values of the metrics in Section 3 among 178 test patterns were $WT_{\mathrm{SI}} = 137$, $WT_{\mathrm{SO}} = 125$ and $WT_{\mathrm{C}} = 14$, respectively. To avoid the invalidation of test results, one has to manage these maximum values during test generation. Tables 1–3 show the test generation results under several power budgets. As power budgets, 90%–10% values of the above maximum values were

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used exclusively, i.e., $(L_{\text{SI}}, \infty, \infty)$ for Table 1; $(\infty, L_{\text{SO}}, \infty)$ for Table 2; and $(\infty, \infty, L_{\text{C}})$ for Table 3 were used. In this experiment, behavioral descriptions that calculate shift-in, shift-out and capture power and that handle various power budgets were automatically created for s1196, and then its gate-level descriptions were derived by a commercial logic synthesis tool. From the results of Tables 1–3, the following remarks can be made.

- Even if only one element of power (shift-in, shift-out, or capture power) is limited, there can be no effect for the other two elements of power.
- Test patterns can slightly increase due to the power limits.
- The capture power limit can be a strong factor for test generation time compared to the other two limits.
- The shift-out power limit can be a strong factor for the detectability of faults compared with the other two limits.

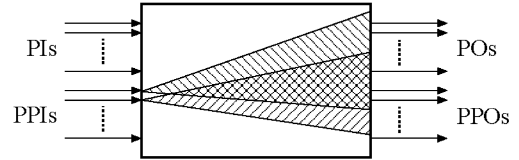
The first remark indicates that one should simultaneously consider all the three elements of power during test generation.

In the second experiment, power-constrained test generation was performed under shift-in, shift-out and capture power limits, simultaneously. As a power budget, $P = (74, 67, 8)$ was given, which is based on the average values of WT_{SI}, WT_{SO} and WT_{C} among 178 test patterns under $P = (\infty, \infty, \infty)$. Row "$P = (74, 67, 8)$" in Table 4 is the test generation result under $P = (74, 67, 8)$. Indeed, we obtained tests that meet the power budget, and completely identified the faults that cause a power violation. However, unfortunately, its test generation time increased drastically. This result indicates that a task to generate tests that meet all the power limits is hard in general. For a large circuit, it would be difficult to achieve complete fault efficiency under a power budget. Some heuristic ideas should be applied to this problem.

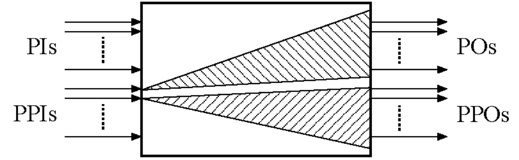
3.3 Heuristic Idea

To overcome the difficulty mentioned above, we present here a heuristic technique using a cone analysis that allows us to have test patterns with low shift-in power.

Now, let us consider logic cones with respect to two or more adjacent PPIs on the scan chain (see Fig. 4). If any two logic cones of them are disjoint, one can treat these adjacent PPIs as one input during test generation. Thereby,



(a) Overlapped cones: Two adjacent PPIs cannot be merged



(b) Disjoint cones: Two adjacent PPIs can be merged

Figure 4: Cone analysis

there are no transitions on the adjacent PPIs when a generated test pattern is shifted-in. Note that, our heuristic idea never degrades fault coverage because the detectability of a fault in one logic cone is independent of the values of the PPIs corresponding to the other logic cones. In other words, although the cardinality of T^f for a fault f in Fig. 1 can be reduced by merging PPIs during test generation, T^f never becomes empty. The problem of identifying such disjoint PPIs as much as possible can be formulated as the clique partitioning problem. By solving its corresponding clique partitioning problem, one can know which PPIs to be merged during test generation. Since the number of PPIs handled during test generation become small by merging PPIs, not only shift-in power can be reduced but also power-constrained test generation can be performed more efficiently. This is because merging PPIs reduce its search space during test generation. It should be noted that, under a given power budget, although the above technique never makes T^f for a fault f in Fig. 1 empty, $T^f_{\text{SI}} \cap T^f_{\text{SO}} \cap T^f_{\text{C}}$ can be empty as a result.

To check the effectiveness of the above heuristic idea, the following experiments were conducted. Row "$P = (74, 67, 8)$ (merge)" in Table 4 gives the test generation result when a power budget was set to $P = (74, 67, 8)$ and the proposed heuristic method was applied. As a result of merging PPIs, 18 PPIs was treated as 10 PPIs during test generation. The result shows that we achieved the same test quality of "$P = (74, 67, 8)$" in much less time. Furthermore, as shown in "$P = (\infty, 67, 8)$ (merge)," we achieved not only the same test quality of "$P = (74, 67, 8)$" but also one order of magnitude reduction in time compared with "$P = (74, 67, 8)$ (merge)," even if shift-in power is not lim-

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Table 1: Test generation results under only peak shift-in power limits for s1196

	Unlimited	$\leq 90\%$	$\leq 80\%$	$\leq 70\%$	$\leq 60\%$	$\leq 50\%$	$\leq 40\%$	$\leq 30\%$	$\leq 20\%$	$\leq 10\%$
#det	3,220	3,220	3,220	3,220	3,220	3,220	3,220	3,220	3,220	3,212
#unt	0	0	0	0	0	0	0	0	0	8
#abt	0	0	0	0	0	0	0	0	0	0
#vec	178	204	216	199	206	201	221	220	202	207
TGT [s]	0.02	0.04	0.36	0.04	0.73	0.22	0.05	0.06	0.03	0.10
Max. WT_{SI}	137	121	77	94	82	68	54	41	25	13
Ave. WT_{SI}	74.76	106.47	67.52	79.29	81.03	66.51	13.72	15.26	9.23	7.11
Min. WT_{SI}	23	88	32	66	65	66	0	0	0	0
Max. WT_{SO}	125	124	118	114	117	111	111	117	111	112
Ave. WT_{SO}	67.16	67.14	66.42	68.80	67.04	67.14	66.48	66.85	67.86	68.32
Min. WT_{SO}	23	23	24	22	19	20	24	23	18	22
Max. CT	14	13	13	15	14	15	13	14	14	14
Ave. CT	8.99	7.96	8.95	10.21	9.38	9.92	9.90	9.68	8.99	9.10
Min. CT	4	3	5	5	3	4	5	3	4	5

ited. The above results indicate the effectiveness of our heuristics.

4 Conclusions and Future Work

In this paper, we proposed a test generation framework to generate stuck-at tests for a scan circuit under peak shift and capture power limits. In terms of completeness, this framework is desirable because one can completely identify whether a fault is testable under a power budget. Unfortunately, however, as demonstrated in Table 4, it is difficult to generate stuck-at tests that meet given limits for shift-in, shift-out and capture power, simultaneously. Every existing test-generation-based method, in a sense, provides one compromise solution between completeness and practicality. We believe that our discussions on completeness and practicality using the framework make it clear where to put one's efforts to seek a good compromise solution. As a good compromise solution, this paper gave a heuristic procedure using a cone analysis that definitely derives tests with low shift-in power and that reduces the search space during test generation. The following points should also be discussed in the future.

- Dedicated test generation technique based on our framework
- Limiter design in terms of circuit size and accuracy of power estimation

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Table 2: Test generation results under only peak shift-out power limits for s1196

	Unlimited	$\leq 90\%$	$\leq 80\%$	$\leq 70\%$	$\leq 60\%$	$\leq 50\%$	$\leq 40\%$	$\leq 30\%$	$\leq 20\%$	$\leq 10\%$
#det	3,220	3,220	3,220	3,199	3,119	3,007	2,832	2,297	2,063	596
#unt	0	0	0	21	101	213	388	923	1,157	2,624
#abt	0	0	0	0	0	0	0	0	0	0
#vec	178	181	175	176	169	161	141	90	67	9
TGT [s]	0.02	0.63	1.74	0.42	0.46	0.42	0.47	0.76	0.74	5.88
Max. WT_{SI}	137	123	130	119	130	135	122	128	118	117
Ave. WT_{SI}	74.76	76.35	77.57	77.32	77.75	76.29	78.31	75.44	77.73	83.78
Min. WT_{SI}	23	26	22	27	22	22	22	22	22	54
Max. WT_{SO}	125	112	100	87	75	62	50	37	25	9
Ave. WT_{SO}	67.16	74.64	68.79	74.64	68.62	47.01	40.47	30.02	21.61	9
Min. WT_{SO}	23	32	32	23	30	19	9	9	9	9
Max. CT	14	14	13	13	14	15	16	14	13	12
Ave. CT	8.99	9.07	9.13	8.93	8.91	8.94	8.88	9.00	9.10	8.78
Min. CT	4	5	4	3	4	4	4	3	5	6

Table 3: Test generation results under only peak capture power limits for s1196

	Unlimited	$\leq 90\%$	$\leq 80\%$	$\leq 70\%$	$\leq 60\%$	$\leq 50\%$	$\leq 40\%$	$\leq 30\%$	$\leq 20\%$	$\leq 10\%$
#det	3,220	3,220	3,220	3,220	3,220	3,220	3,220	3,220	3,220	3,219
#unt	0	0	0	0	0	0	0	0	0	1
#abt	0	0	0	0	0	0	0	0	0	0
#vec	178	200	196	200	188	193	194	186	186	187
TGT [s]	0.02	0.18	0.12	0.07	0.31	1.40	0.05	27.57	0.11	0.49
Max. WT_{SI}	137	79	129	119	80	137	131	99	113	115
Ave. WT_{SI}	74.76	25.71	81.47	72.69	31.30	74.39	70.95	51.44	70.26	68.31
Min. WT_{SI}	23	0	22	14	0	28	18	0	13	20
Max. WT_{SO}	125	124	110	134	124	124	126	119	124	111
Ave. WT_{SO}	67.16	70.11	63.31	66.41	70.48	62.65	65.53	70.70	63.40	61.16
Min. WT_{SO}	23	19	9	26	19	24	24	9	24	24
Max. CT	14	12	11	9	8	7	5	4	2	1
Ave. CT	8.99	8.38	9.21	8.48	8.00	3.56	4.48	4.00	1.88	0.61
Min. CT	4	4	8	8	8	0	4	4	0	0

Table 4: Test generation results under peak power limits

Case	#det	#unt	#abt	#vec	TGT [s]	Max.		
						WT_{SI}	WT_{SO}	CT
$P = (\infty, \infty, \infty)$	3,220	0	0	178	0.02	137	125	14
$P = (74, 67, 8)$	3,038	182	0	174	17,132.35	74	67	8
$P = (74, 67, 8)$ (merge)	3,038	182	0	177	161.30	41	67	8
$P = (\infty, 67, 8)$ (merge)	3,038	182	0	169	15.02	53	67	8

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