Advanced Datapath Synthesis Incorporating Intentional Timing Skew for High Performance Nanometer VLSIs

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Abstract

In the logic level VLSI design, the clock skew is now utilized intentionally for improving system performances and significant efforts have been devoted. Similar to the clock schedule in the logic level design, the skew-aware high level design will contribute to reducing the clock period. In addition, the intentional skew considered in high level synthesis may also contribute to reducing the number of control steps (makespan) for a target application. In the logic level design, the effect of the intentional clock skew is often enhanced by re-timing technique. Similar to this situation, in the skew-aware high level synthesis, the simultaneous optimization of the control step assignment and the skew assignment has a higher potential in performance optimization.

In this thesis, we investigate the optimization of schedule (σ), skew (τ) and clock period (clk). We assume that resource binding and delay information are given as an a part of input description. The contributions of this thesis are following.

- The proof of NP-hardness of simultaneous optimization of (σ,τ,clk).
- The proof of NP-hardness of simultaneous optimization of (σ,τ) under given clk.
- The proof of NP-completeness of decision problem whether there exists a feasible pair of (σ,τ) for the input instance under given clk.
- A sufficient and necessary condition for the input instance to have a feasible pair of (σ,τ) for any clk. This condition is also a sufficient condition to have a feasible pair of (σ,τ) for specified clk.
- A heuristic algorithm for simultaneous optimization of (σ,τ) under given clk. The objective of the algorithm is to minimize the number of control steps.

Intentional skew control is a promising key technology not only to improve VLSI performance, but also to provide tunability for each VLSI to operate with its own maximum performance, which may overcomes the current and future process variability problem.

Those results presented in this paper should be important theoretical base of skew-aware datapath design.

Key Words: Skew optimization, High Level Synthesis, Scheduling