

Title	矩形パッキングとそのVLSIモジュール配置問題への応用
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Citation	
Issue Date	1997-03
Type	Thesis or Dissertation
Text version	author
URL	http://hdl.handle.net/10119/833
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Description	Supervisor:岡本 栄司, 情報科学研究科, 博士

Rectangle Packing and Its Applications to VLSI Module Placement Problem

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January 16, 1997

Abstract

The first and the most critical stage in VLSI layout design is the placement. The background of which is the *rectangle packing problem* : Given a set of rectangular modules of arbitrary sizes, place them without overlap on a plane within a rectangle of minimum area. Since the variety of the packing is uncountably infinite, the key issue for successful optimization is the introduction of a finite solution space which includes an optimal solution and excludes all the infeasible solutions. The main contribution of this thesis is in the introduction of such a solution space where each packing is represented by a pair of module name sequences, called *sequence-pair*. The introduction of this solution space enables us to use stochastic optimization method such as standard simulated annealing, and it is demonstrated that hundreds of modules have been packed very efficiently. The biggest MCNC benchmark example is also shown to be placed very promisingly with a conventional wiring consideration method.

Although module positions are successfully represented by the sequence-pair, it is desired frequently in VLSI design that channels are represented together with modules, because a channel router is often used in the following routing stage. For this request, this thesis gives a mapping from a sequence-pair to a rectangular dissection, which represents channels by line segments.

Placement with obstacles in the chip is also discussed in this thesis, for dealing with pre-placed modules and with a rectilinear placement region. The obstacles are easily included in a sequence-pair to eliminate the overlaps, but the sequence-pair cannot be responsible to recover the assigned coordinates of the obstacles. To solve this practical problem, this thesis gives an algorithm which changes an inconsistent sequence-pair for a consistent one.

Key Words: Rectangle packing, Solution space, VLSI module placement