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Shifted Recursive Torus: An Interconnection Network for Massively Parallel Computers

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Abstract

Multiprocessor systems consisting of millions of processing elements have been expected to solve advanced scientific and engineering problems in the next decade. Since the interconnection network is one of the critical components of multiprocessor systems, they are required network feature such as smaller diameter, easy VLSI implementation, fault-tolerant schemes, and good expandability. In this paper, we propose Shifted Recursive Torus (SRT) interconnection network for scientific computing, and discuss network performance, routing algorithms, and fault-tolerant schemes. The SRT is constructed by adding hierarchical multi-level links to the torus network. To keep a network degree be small, levels are assigned to node exclusively. Since the SRT has no diagonal links, the SRT can be easily implemented in VLSI and achieve fault-tolerances by a simple scheme.

First, we describe a basic structure of one dimensional SRT (1D-SRT) and prove that the degree of 1D-SRT is always less than four. The diameter and the wiring area is theoretically derived. A recursive algorithm is proposed for routing of the 1D-SRT and achieves the good routing performances. Network features of the 1D-SRT are compared with those of other networks. Although the degree of 1D-SRT is almost the same as the Chordal Ring, the diameter of SRT is much smaller than that of the Chordal Ring.

Next, we expand the 1D-SRT to two dimensional SRT (2D-SRT). We derive connection rules of the 2D-SRT and propose an uniform 2D-SRT to improve the communication performance. The recursive routing algorithm of the 1D-SRT is extended for 2D-SRTs and it can perform in $\mathcal{O}\left(2\sqrt{\log_2 N}\sqrt{\log_2 N}\right)$ steps on the 2D-SRT consisting of $N \times N$ nodes. Parallel FFT on the 2D-SRT is discussed by embedding the data structure into the 2D-SRT. Comparing network features with conventional networks such as RDT, DTN and hypercube, the SRTs have good network performances for massively parallel computers.

In order to implement SRTs in WSI, we propose fault-tolerance schemes which use bundle of links, simple switches, and spare nodes. We also evaluate temperature distribution of wafer stacks by thermo-conducting simulations and discuss system yields of SRTs.

Key Words: **massively parallel computer, interconnection network, torus network, mesh network, routing algorithm**