Disturb-Free Writing Operation for Ferroelectric-Gate Field-Effect Transistor Memories With Intermediate Electrodes

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***Abstract*—To achieve disturb-free writing, we proposed a new writing operation for ferroelectric-gate field-effect transistor memories with intermediate electrodes. The writing voltages V_W applied to the wordlines for Pr^+ and Pr^0 memory states are the same pulse magnitudes, which consist of V_W^+ followed by V_W^-, whereas the bias timings of the bitline voltages differ from each other. The bitline voltage for the Pr^+ memory state is set high when V_W is set V_W^+, and it is set to low by the time when V_W is changed to V_W^-. On the other hand, the bitline voltage for the Pr^0 memory state is set high until the whole writing pulse of $(V_W^+ + V_W^-)$ is finished. This is verified experimentally using a discrete circuit, which showed that the new writing operation achieves disturb-free writing. The memory consists of two transistors for data writing and reading. With the obtained experimental results, we discuss the possibilities of high integration of this memory as well as low reading voltage.**

***Index Terms*—Disturb free, ferroelectric-gate memory, ferroelectric memory, nondestructive readout, write disturbance.**

I. Introduction

FERROELECTRIC-GATE field-effect transistor (F-FET) memories are known to be one of the ultimate nonvolatile memories because of their remarkable features, such as nondestructive readout, high packing density, high reading speed, and low power consumption [1], [2], compared with ferroelectric random-access memories (FeRAMs). Furthermore, they have the advantages of low writing voltage, fast writing speed, and high endurance, compared with flash memories [3]. Although considerable researches on F-FET memories have been carried out [4]–[7], F-FET memories have not been commercialized because of problems such as short retention time [8], [9] and high writing voltage [10], [11]. To overcome these problems, we have proposed a new F-FET memory (denoted as IF-FET memory), in which an intermediate electrode (IE) for data writing is inserted between the ferroelectric capacitor C_f and the buffer layer (the gate) of a reading MOSFET (R-MOSFET) [13]–[15]. For data writing, using the IE, a writing voltage V_W is applied directly to the C_f without voltage dropping on the buffer layer, and for data reading, a reading voltage V_R is applied between the top of C_f and the source of R-MOSFET with the IE being electrically floated. The memory needs another MOSFET for data writing in addition to R-MOSFET. The detailed configuration is given in Section II. Recently, we have also proposed an improved reading operation for perfect nondestructive readout [16]. In this operation, we used two kinds of memory states, a positive remanent-polarization Pr^+ state and a nearly nonpolarized Pr^0 state in C_f. For data reading, following a positive reading pulse with the magnitude V_R^+ to decode the memory state of C_f, a negative reading pulse with the magnitude V_R^- is applied to return the readout memory state to the initial one. It was confirmed experimentally that this reading operation improved the readout endurance more than 10^8 reading cycles and the retention time to exceed ten years [16], using a discrete circuit of IF-FET memory or one memory cell. It can be expected that the nondestructive readout by this operation endures until ferroelectric properties of C_f are degraded intrinsically such as fatigue and imprint. High endurance is another advantage of IF-FET over 1-transistor–1-capacitor (1T–1C) FeRAM in addition to the previously mentioned advantages of F-FET, except for that with high packing density. The high endurance results from the use of minor polarization-electric field $(P$–$E)$ loops for data reading instead of full switching of polarization like that in FeRAM, which is explained in detail later. Ishiwara *et al.* proposed a 1-transistor–2-capacitor (1T–2C), whose operation principle is similar to IF-FET, as a substitute of conventional F-FET. The total area of 2C in 1T–2C cannot be reduced to and overlapped with the gate area of R-MOSFET, which is not suitable for high integration of the memory. On the contrary, C_f of IF-FET can be fabricated just on the gate with the same area. The other comment on comparison with 1T–2C has been mentioned before [12].

However, disturbance of data in the writing operation (write disturbance) of IF-FET occurs in the case of memory array structure of an integrated circuit, which is a serious problem for practical use. We propose a new writing operation of IF-FET after demonstrating the problem related to a previous writing operation. By using a discrete circuit, we have also verified experimentally that the new writing operation is write disturb free as compared with the previous one. Finally, with the obtained results, we discuss the integration of IF-FET and the related issue of reading voltage.

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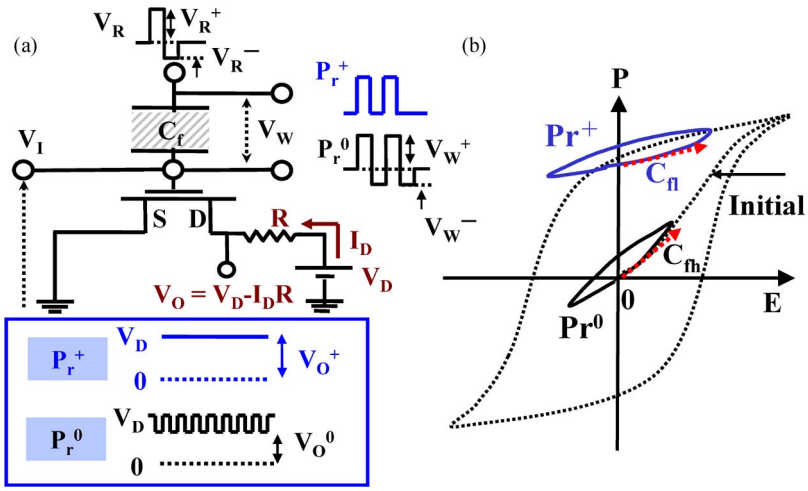

Fig. 1. (a) (Top) Schematic equivalent circuit of the IF-FET memory, and (bottom) output voltages V_O^+ and V_O^0 for Pr^+ and Pr^0 memory states, respectively, corresponding to the continuous reading pulse V_R. (b) Schematic P–E hysteresis loop and initial curve (dotted lines) of a ferroelectric capacitor C_f. (Solid lines) Minor loops that originate from Pr^+ and Pr^0 are traces of P–E in data reading. The C_{fl} and C_{fh} are the capacitance values of Pr^+ and Pr^0 states, respectively, in the positive E.

II. Problem and Improvement of Data Disturbance

Fig. 1(a) shows a schematic equivalent circuit of IF-FET memory, which consists of a ferroelectric capacitor C_f connected serially to an n-channel R-MOSFET. In this figure, an output voltage V_O is measured on a resistor R at the drain of the MOSFET, which is biased by a dc voltage V_D. As memory states, we use a positive remanent polarization Pr^+ and a nearly nonpolarized Pr^0. Fig. 1(b) shows not only the schematic P–E hysteresis loop and initial P–E curve (dotted lines) but also the two minor loops (solid lines). The minor loops represent the P–E traces during IF-FET reading operation for the Pr^+ and Pr^0 memory states. C_{fl} and C_{fh} are denoted as ferroelectric capacitances of Pr^+ state and Pr^0 state, respectively, which are values in response to the positive rising pulses for data reading. Because C_f is proportional to the gradient of the P–E slope, the C_{fh} of Pr^0 is larger than the C_{fl} of Pr^+. The outline of the previous operation is as follows: Both memory states are produced by applying writing voltages directly to the C_f, where the drains are grounded at $V_D = 0$. The writing voltage V_W for Pr^+ state was a positive square pulse, and V_W for Pr^0 state was a combined square pulse consisting of a positive pulse magnitude V_W^+ followed by a negative pulse magnitude V_W^-, as shown in Fig. 1(a). V_W^+ is to reset the previous stored memory state, and V_W^- is to determine the polarization of Pr^0 state. For data reading, a reading voltage consisting of a positive pulse magnitude V_R^+ followed by a negative pulse magnitude V_R^- is applied between the top of C_f and the ground, where the IE is electrically floated and the drain is biased by a positive V_D. Therefore, the reading voltage V_R is applied to C_f and C_i in series, and it is divided into two voltage drops of V_f on C_f and V_I on C_i, where C_i is an input capacitor of the R-MOSFET. Because V_I or IE voltage of Pr^+ state is lower than that of Pr^0 state, which is due to $C_{\mathrm{fl}} < C_{\mathrm{fh}}$, a drain–current I_D of the R-MOSFET in the Pr^+ state is much smaller than that in the Pr^0 state. The reading V_R^+ is required not to be as high as to saturate polarization like FeRAM but to produce a detectable difference in I_D. The memory states can be distinguished by measuring a difference in $V_O = V_D - I_D\mathrm{R}$, $\Delta V_O = V_O^+ - V_O^0$, between V_O^+ for Pr^+ state and V_O^0 for Pr^0 state.

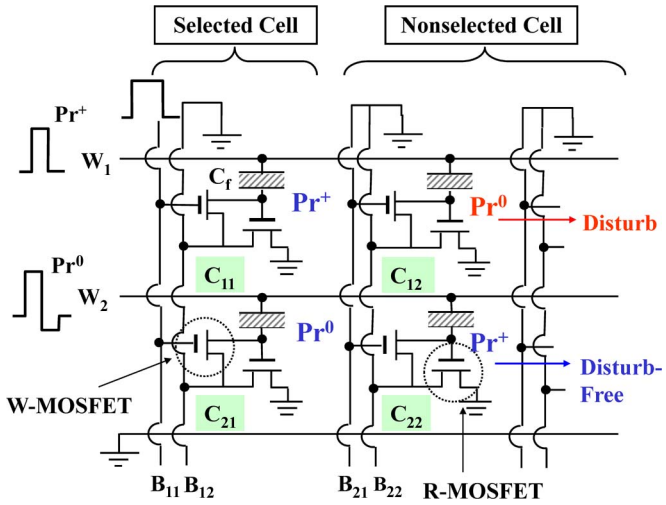

Fig. 2. Previous writing operation for an integrated array of IF-FET memory cells. A writing voltage for Pr^+ memory state is a positive pulse and that for Pr^0 memory state is a combined pulse consisting of a positive pulse followed by a smaller negative pulse. For data writing, the W-MOSFETs in the selected cells are turned on to apply the writing voltages directly to the C_f. This operation causes write disturbance of Pr^0 memory states because the Pr^+ writing voltage is positive.

Figs. 2 and 3 show the schematic arrays of IF-FET memory cells for the previous writing operation and the proposed writing operation, respectively, in integrated circuits. In each memory cell, an additional writing MOSFET (W-MOSFET) is used as a switch to short-circuit the R-MOSFET to the ground for data writing. The W-MOSFETs are integrated for the selection of writing cells. For large-scale integration, this configuration seems unsuitable because a 1C–2T occupies a large area. However, in an actual integrated circuit, the capacitor can be fabricated just over the gate of R-MOSFET, the area being the same as the gate. Therefore, the configuration of IF-FET memory consists of two transistors (2T memory) in

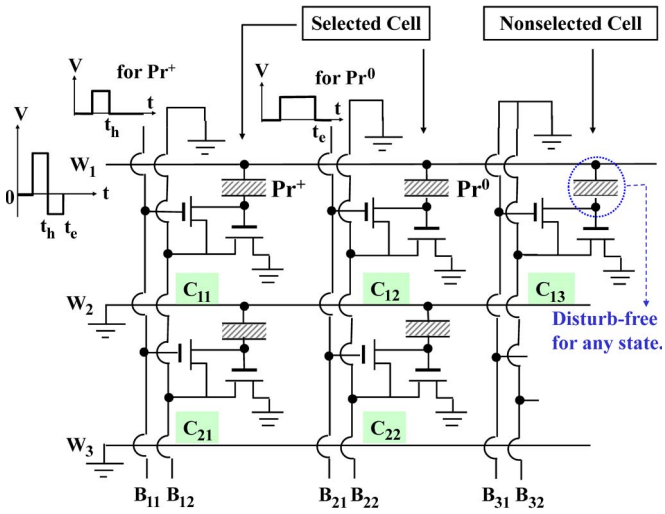

Fig. 3. Proposed writing operation for an integrated array of IF-FET memory cells. The writing voltages to the wordlines for Pr^+ and Pr^0 memory states are the same. They are combined pulses consisting of a positive pulse magnitude V_W^+ followed by a negative pulse magnitude V_W^-, where the switching time from V_W^+ to V_W^- is t_h and the end time of the writing voltage is t_e. The bitline switching times from high to low for the Pr^+ and Pr^0 states are before t_h and after t_e, respectively. Using this operation, write disturb free is achieved.

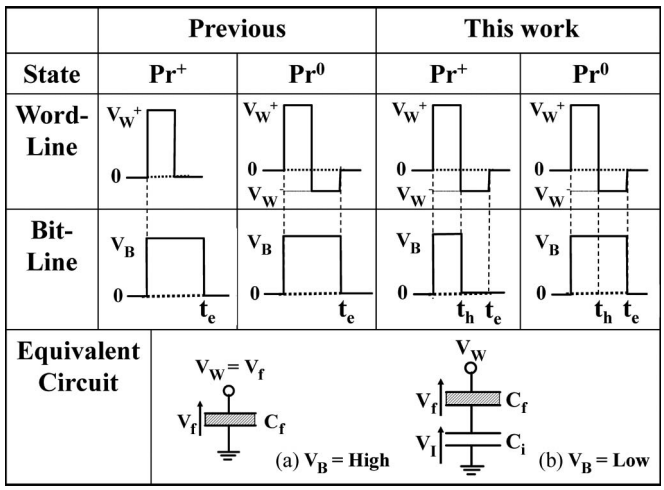

Fig. 4. Comparison of bias timings in wordline and bitline between the previous and proposed writing operations, for Pr^+ and Pr^0 memory states. The bottom shows the equivalent circuits of the memory cells for (a) high bitline and (b) low bitline in writing operation. t_e and t_h are explained in the caption of Fig. 3.

practice. This issue is further discussed later. Fig. 4 also shows the comparison of bias timings of wordline and bitline pulses between the previous and the proposed writing operations, for Pr^+ and Pr^0 memory states. In the previous case, the wordline pulses for Pr^+ and Pr^0 states are different from each other, and the bitline pulses are the same but vice versa in the proposed case. The bottom figures in Fig. 4(a) and (b) show the equivalent circuits for high and low bitline voltages, respectively, of the memory cells in writing operation. When bitlines are high, the W-MOSFETs are ON-state, and the writing voltages are applied directly to C_f. When bitlines are low, the W-MOSFETs are OFF-state, and the writing voltages are applied to C_f and C_i in series, which is similar to a readout case.

The previous writing operation is explained using Figs. 2 and 4. By setting the bitline B_{11} high and applying the writing voltages of Pr^+ and Pr^0 to the wordlines W_1 and W_2, respectively, the C_{11} and C_{21} cells store Pr^+ and Pr^0 memory states, respectively, where the B_{12} line is grounded. By this writing operation, the memory cells can be taken as the equivalent circuits of Fig. 4(a). The nonselected cells with the ground bit lines (e.g., the C_{12} of Pr^0 and C_{22} of Pr^+) are also applied by the writing voltages of Pr^+ and Pr^0, respectively, and some voltages V_f drop on the C_f's, as shown in Fig. 4(b) of the equivalent circuit. For the case of Pr^0 writing, the C_{22} of Pr^+ memory state remains because the waveform of the writing pulse of Pr^0 is similar to that of a nondestructive reading voltage. This is write disturb free. However, for the case of Pr^+ writing, the memory state of C_{12} changes from the Pr^0 state toward a Pr^+ state because of the application of the positive writing voltage. This is a severe write disturbance. Needless to say, the other disturbances of Pr^+ state due to Pr^+ writing and of Pr^0 state due to Pr^0 writing are free.

To improve write disturbance of Pr^0 state due to Pr^+ writing, we propose a new writing operation. When we write a Pr^+ memory state, we use the previous writing voltage for Pr^0 instead of Pr^+, which is possible by means of controlling bias timing of bitline voltages, as shown in Figs. 3 and 4. In Fig. 3, the operation sequences are explained for the two cases of writing Pr^+ and Pr^0 memory states into the C_{11} and C_{12} cells, respectively. For the C_{11} cell, the high voltage of the B_{11} line has fallen down to the ground before the writing voltage changes from V_W^+ to V_W^- at t_h. With this operation, the C_{11} cell can be stored as a Pr^+ state because the positive V_W^+ drops on only C_f until t_h, as shown by the equivalent circuit in Fig. 4(a), and then, V_W^- drops on the C_f and C_i in series until t_e, as shown by the equivalent circuit in Fig. 4(b). Because the bias condition on the C_f and C_i is the same as the nondestructive readout case, the Pr^+ state written by V_W^+ remains even after the application of V_W^-. On the other hand, for the C_{12} cell, the voltage of the B_{21} line does not fall down to the ground until t_e in which the whole writing pulse is finished. By this operation, the C_{12} cell can be written into as a Pr^0 state. Because the waveform of the writing voltage is the same as the nondestructive reading voltage, the nonselected memory cell (e.g., C_{13}) is free from write disturbance.

III. Experimental Setup

We examined the write disturbance using a discrete circuit, as shown in Fig. 1(a). First, a Pr^+ or Pr^0 state was written into the C_f by applying the writing voltage between the top and the IE, where the voltage had double periods to produce a steady memory state without writing errors. Next, we disturbed the stored memory by applying writing voltages between the top electrode and the ground continuously, floating the IE electrically. This bias condition could be taken as a write-disturbance situation of a nonselected cell in an integrated circuit. The number of writing times was varied from 10^0 to 10^8, where one time was one period. After that, by measuring V_O, we estimated the disturbance characteristics of the stored memory state. The sample structure of C_f consisted of (RuO_x :

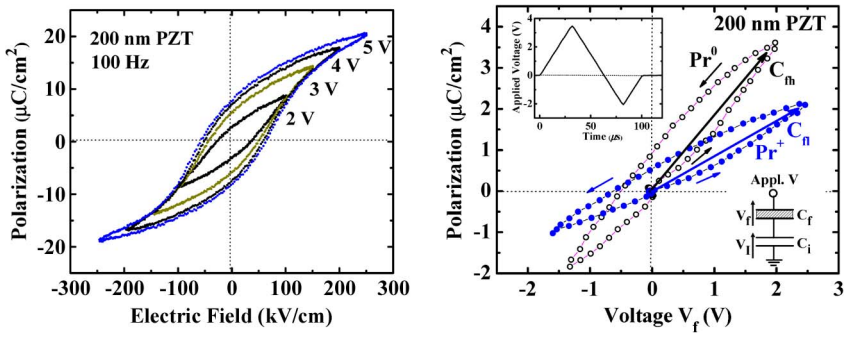

Fig. 5. (a) P–E hysteresis loops at 100 Hz of the PZT film used in this paper. (b) Relationships between the polarizations P and applied voltages V_f to the PZT film for Pr^+ and Pr^0 memory states in the similar condition of reading operation. The lower inset is the equivalent circuit of Fig. 1 at $V_D = 2.0$ V for this measurement. The upper inset shows the applied voltage V of a modified triangular waveform. From this, it can be seen that the C_{fh} is about twice as large as the C_{fl}.

top electrode)/PtO_x/PZT/Pt/(RuO_x : bottom electrode) on an SiO_2/Si substrate. The ferroelectric layer was a 200-nm-thick and highly (100)/(001)-oriented PZT film, and the top electrode diameter D_t was 100 μm. The R-MOSFET was a commercial version of 2SK679A with $C_i = 180$ pF, V_D was 2 V, and R was 2 kΩ. The pulsewidths of V_W^+, V_W^-, V_R^+, and V_R^- were 50 μs, and the one period for data writing and data reading was 100 μs. Although it is not necessary for the writing period to be very long in the light of domain switching time and time constant of the measurement circuit, we allowed it to coincide with the reading one.

Fig. 5(a) shows the P–E hysteresis loops of the used PZT film, which were measured by a Sawyer–Tower circuit with a sine wave at 100 Hz. It can be observed that the P–E loops become saturated for applied voltages higher than 4 V. Thus, we set $V_W^+ = 4$ V, and the Pr^+ memory state had a positive remanent polarization near 4 V, as shown in Fig. 5(a). For clear readout by application of V_R^+, the gate voltage of the R-MOSFET V_I for the Pr^+ memory state should be equal to or a little smaller than the threshold voltage of the MOSFET, $V_{\mathrm{th}} = 1.4$ V. Therefore, we set V_R^+ to be 3.5 V, taking account of C_{fh}, C_{fl}, C_i, and V_{th}. The actual values of C_{fh} and C_{fl} are mentioned later. Application of V_W^- following V_W^+ for data writing is to produce a Pr^0 memory state from the Pr^+ state produced by V_W^+. The polarization of the Pr^0 should be near the origin of the P–V hysteresis loop from two viewpoints of nondestructive readout and clear difference in output from the Pr^+ memory state. In addition, application of V_R^- has an important role to return any readout memory state to the initial memory state for the purpose of nondestructive readout. Because the optimum V_W^- and V_R^- depend on the properties of C_f and R-MOSFET and are related with each other, we determined them experimentally. Through the process mentioned as in the previous report [16], we set $V_W^+ = 4.0$ V, $V_W^- = -2.3$ V, $V_R^+ = 3.5$ V, and $V_R^- = -2.0$ V as the optimum pulse magnitudes in this paper.

Fig. 5(b) shows the relationships between the polarization P of the PZT film and the applied voltage V_f to the film for the Pr^+ and Pr^0 memory states. For this measurement, the circuit shown in Fig. 1 was used at $V_D = 2.0$ V, and the equivalent circuit is shown in the lower inset of Fig. 5(b). The applied voltage was a modified triangular waveform as also shown in the upper inset of Fig. 5(b). The maximum and minimum voltages were 3.5 and -2.1 V, respectively; the duration times of the positive and negative voltages were 62.5 and 37.5 μs, respectively; and the total or one periodic time was 100 μs. The maximum and minimum voltages and the total time were matched with the actual reading conditions of V_R^+, V_R^-, and one period, respectively. The duration times were unintentionally controlled because of the equipment specification, and their exact values are not physically important for this paper. The polarization P was calculated by the formula of $P = 4V_I \cdot C_i/(\pi D_t^2)$, and V_I was measured by an oscilloscope whose probe had the input resistance and capacitance of $R_p = 10$ MΩ and $C_p = 10$ pF, respectively. Because $C_i = 180$ pF was much larger than C_p and the time constant $R_p(C_i + C_p) = 1900$ μs was much larger than 100 μs, the input impedance of the oscilloscope can be ignored for this measurement. From this figure, it is shown that the curve slope of the Pr^+ state is lower than that of the Pr^0 state, and the capacitances of the PZT film for the Pr^+ and Pr^0 states are estimated to be $\sim$70 and $\sim$140 pF, respectively. It is also shown that both the P–V curves return to the measurement starting point or the origin after the one periodic measurement, which are similar to the minor loops shown in Fig. 1(b). This implies that nondestructive readout is possible in IF-FET.

To produce Pr^+ memory states by the new writing operation in a discrete circuit, we added another MOSFET (W_d-MOSFET) to the circuit of Fig. 1(a), as shown in the inset of Fig. 6(a). The source, gate, and drain of the W_d-MOSFET were connected with the ground, the top electrode of C_f, and the IE, respectively. When the pulse magnitude of the new writing voltage is a positive V_W^+ applied between the top electrode and the ground, the W_d-MOSFET is set to the ON-state so that a Pr^+ state is written into the C_f. When the pulse magnitude changes to a negative V_W^-, the W-MOSFET was set to the OFF-state so that the V_W^- was applied on the C_f and C_i in series. By this operation, the Pr^+ memory state written by V_W^+ remains because this writing operation is effectively equivalent to nondestructive readout operation. As a W_d-MOSFET, we used the same commercial MOSFET as the R-MOSFET. To write a Pr^0 memory state, the writing voltage was applied directly to the C_f

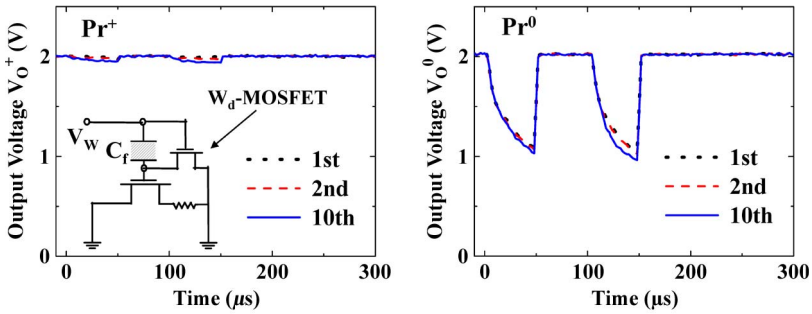

Fig. 6. Nondestructive readout characteristics for (a) the Pr^{+} state and (b) the Pr^{0} state, using the writing pulse magnitudes of $V_W^+ = 4.0$ V and $V_W^- = -2.3$ V, and the reading pulse magnitudes of $V_R^+ = 3.5$ V and $V_R^- = -2.0$ V. The numbers of readout times are the first, second, and tenth, where the retention or interval time is 1 min after each readout. The W_d-MOSFET was used only for writing Pr^{+} memory state, which is not needed in integrated circuits.

without using W_d-MOSFET. After experimentally confirming the nondestructive readout of the memory states written by the new writing operation, we investigated the write-disturbance characteristics.

IV. Results and Discussion

Fig. 6(a) and (b) shows the nondestructive readout characteristics for the Pr^{+} and Pr^{0} memory states, respectively. The memory state after each readout from the first to the tenth time was retained for 1 min under the condition that the IE was electrically floated and that the top electrode and the source and drain of the R-MOSFET were grounded. For every reading operation, the double periodic reading voltages were used. We can see that the characteristics for the Pr^{0} state, as well as those for the Pr^{+} state, show almost the same as any readout time. Then, the output difference ΔV_O constantly remains approximately 1 V through all of the readout times. However, V_O for the Pr^{+} and Pr^{0} states are decreased slightly with the readout times, and the V_O for the second reading pulses are always lower than the first ones for any readout time. We can speculate possible causes for this phenomenon as follows: The negative pulse magnitude V_R^- of the reading voltage was adjusted so that the memory state could return to the initial memory state from the readout state by V_R^+. Because this adjustment was performed by only one readout time with one periodic reading voltage, the domain or polarization state of the C_f might not become steady state, compared with readout memory states subjected to more readout operations. Therefore, some amount of negative domains or upward domains might be increased a little from the initial memory state by repeating the readout operation. Because we obtained nondestructive readout endurance over 10^8 cycles as previously reported [16], it can be considered that the increment in volume of upward domain per one readout time is very small and is rapidly decreased with the number of readout times. Therefore, we can read out nondestructively the IF-FET memory written by the new writing operation. It is also noted that the response of V_O is slow to the V_R^+ pulse particularly in the Pr^{0} state. This is not due to the circuit time constant (i.e., $(C_f//C_i)\cdot R$) because the time constant is approximately 0.2 μs and much smaller than the pulsewidth of 50 μs. The main reason may be the requirement of some time to switch polarization domains, whose dynamics are governed by nucleation and growth of the ferroelectric domain [17]–[20]. It has been reported that the volume fraction $\Delta P(t)/\Delta P(\infty) = p(t)$ of the switched domain, which is dependent of switching time t, can be described by $p(t) = 1 - \exp[(-t/t_0)^n]$. $\Delta P(t)$ is a switched polarization at t, and $\Delta P(\infty)$, which strongly depends on an electric field E_f in C_f, is a saturation of switched polarization at infinite time. t_0 and n are called the characteristics switching time and dimensionality, respectively, of the growing domains. It is well known that t_0 depends on E_f, crystal defect, grain size, electrode material, and so on. For example, Tagantsev *et al.* reported that $p(t)$ was approximately 80% at $t = 1$ ms for a 135-nm-thick (111)-textured PZT film with an IrO_x top electrode and $E_f = 100$ kV/cm [17]. In our case, E_f was approximately 100 kV/cm, and the switching time was approximately 50 μs. Because V_I is proportional to $\Delta P(t)$, it varies with t corresponding to $p(t)$. Furthermore, by the transconductance g_m of the R-MOSFET and R, an infinitesimal intermediate voltage or gate voltage δV_I is amplified inversely to an infinitesimal output voltage $\delta V_O = -\delta V_I \cdot g_m \cdot R$. Therefore, it was observed that the response of V_O^0 for Pr^{0} was fairly slow as shown in Fig. 6(b), compared with the V_R^+ square pulse. If E_f is increased by increasing V_R^+, we can obtain much faster response because it has been reported that t_0 follows an experimental low of $t_0 \infty \exp(\alpha/E_f)$ [19], [21], where α is called as the activation field. Increasing V_R^+, however, probably leads to higher power consumption. Because ferroelectric films have a high potential of domain switching time of a few nanoseconds [22]–[24], an operation time of IF-FET can be reduced to nanosecond order by improving the material properties of the ferroelectric film and electrode and the process techniques.

Fig. 7(a) shows the write-disturbance characteristics of Pr^{0} memory state due to the previous writing operation. In this case, V_W for Pr^{+} is 4.0 V, $V_W^+ = 4.0$ V, $V_W^- = -2.3$ V, $V_R^+ = 3.5$ V, and $V_R^- = -2.0$ V. From this figure, it can be seen that the output voltage V_O^0 for the Pr^{0} write disturbance remains almost constant during the measurement, which means that there is no write disturbance, as expected. However, the V_O^0 for the Pr^{+} writing disturbance quickly increases with the number of writing times. V_O^0 of the initial memory state before the Pr^{+} write disturbance was approximately 0.9 V, which was almost equal to V_O^0 of the Pr^{0} writing disturbance. This means that the memory state is destroyed and that severe write disturbance

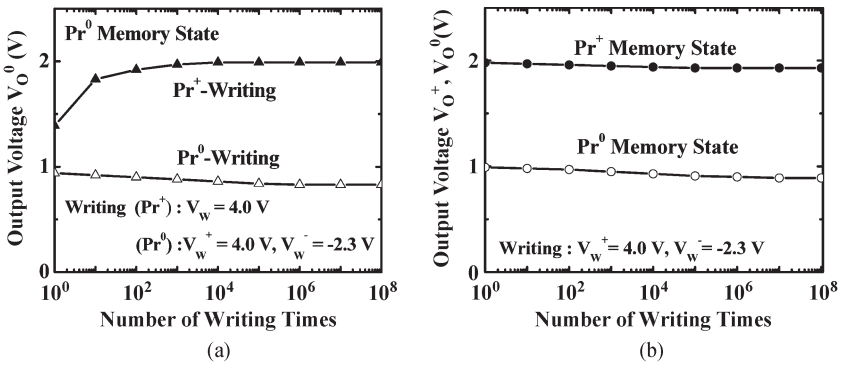

Fig. 7. (a) Write-disturbance characteristics of Pr^0 memory state due to the previous writing operation, in which the writing voltages for Pr^+ and Pr^0 states are different from each other. The Pr^+ write disturbance is severe, although the Pr^0 write disturbance is almost free. (b) Write-disturbance characteristics of Pr^+ and Pr^0 memory states due to the writing operation proposed in this paper, in which the writing voltages for both states are the same.

occurs. This is because the positive writing voltages V_W were applied continuously to the stored Pr^0 memory state, which was changed toward a positive polarization from nearly neutral. For the Pr^+ memory state, write disturbance due to both the Pr^+ and Pr^0 writing operations was not observed.

Fig. 7(b) shows that there were no write disturbances due to the new writing operation for both memory states. Strictly speaking, the V_O for both memory states are slightly decreased with the number of writing times. The same behavior is observed on V_O^0 due to the Pr^0 writing disturbance shown in Fig. 7(a). This is because the polarizations of both the memory states may gradually change from the initial states according to the number of writing times in the final steady state, as shown in Fig. 6. The variations are so small to be negligible for the memory operation, and there is room to improve them further by adjusting the ferroelectric property of C_f and the writing and reading pulse magnitudes [16]. Thus, from the results shown in Fig. 7(b), it can be said that the new writing operation is effective for write disturb free in IF-FET memory.

Finally, we discuss the integration issue of IF-FET. As previously mentioned, one ferroelectric capacitor (1C) of IF-FET can be formed directly on the gate oxide layer of R-MOSFET, the area of 1C being the same as that of the R-MOSFET gate. Under this condition of area, it is examined whether an operation voltage of IF-FET is reliable or not for commercialization. We estimate threshold reading voltages V_{TR}^+ for Pr^+ state and V_{TR}^- for Pr^0 state, at which V_I is equal to V_{th} of R-MOSFET. They are given by the following simple formulas [14]:

$$V_{\mathrm{TR}}^+ = \left[\left(\frac{C_i}{C_{\mathrm{fl}}}\right)+1\right]V_{\mathrm{th}} \quad V_{\mathrm{TR}}^- = \left[\left(\frac{C_i}{C_{\mathrm{fh}}}\right)+1\right]V_{\mathrm{th}}. \quad (1)$$

The assumptions for the estimation are as follows: The gate structure is metal/100-nm-thick ferroelectric/metal/3-nm-thick SiO_2 on Si in IF-FET, and V_{th} is 1.0 V. The relative dielectric constants of C_i, C_{fl}, and C_{fh} are 3.9, 200, and 400, respectively, according to the result shown in Fig. 5(b). Under this condition, we obtain $V_{\mathrm{TR}}^+ = 1.65$ V and $V_{\mathrm{TR}}^- = 1.33$ V. Because the difference between them is approximately 0.3 V, and the operation voltage can be less than 1.5 V, we can realize an IF-FET with the gate-stacked structure of metal/ferroelectric/metal/SiO_2. If a connection terminal of the IE is extended not from the edge of the source or drain but from the side in the channel width direction, self-align process may be available at the expense of a small additional area. Thus, the actual area of IF-FET cell in integrated configuration is occupied roughly by 2T. We can reduce the occupied area if the 2T share the source or drain region in common. In static RAMs, thin-film transistors (TFTs) of polycrystalline Si are stacked over MOSFETs fabricated on a Si substrate to reduce the area per one memory cell [25]–[27]. If TFTs for W-MOSFETs are stacked over R-MOSFETs in integrated IF-FET, the packing density can be much increased. The drawback of IF-FET integration is technical complexity, such as fabrication of stacking TFTs over R-MOSFETs and the IEs between C_f and C_i, which induces high cast. This problem may be eased somewhat if the stacked layers (e.g., TFT) are fabricated at temperature lower than 400 °C. Low-temperature fabrication processes can reduce serious degradation of material properties (e.g., ferroelectric properties of C_f) in the under layers.

V. Conclusion

We have proposed a new operation for disturb-free writing in IF-FET memories. When Pr^+ and Pr^0 states are written into memory cells, wordlines are applied by the same writing voltages consisting of a positive pulse magnitude V_W^+ followed by a negative V_W^-, whereas the bitlines are applied by voltages that differ from each other. For the Pr^+ state, the bitline voltage falls down from high to low before the writing pulse magnitude changes from V_W^+ to V_W^-. On the other hand, for the Pr^0 state, the bitline voltage decreases when the whole writing voltage is finished. Because the waveform of the new writing voltage is similar to that of nondestructive reading voltage, IF-FET memory can be free from write disturbance. In fact, using the discrete circuit, we verified the usefulness of the new writing operation, showing disturb-free writing for any memory state for at least 10^8 writing times. Furthermore, we discussed the possibility of the high integration of IF-FET and estimated the reading voltage that would be sufficient for the commercialization of IF-FET using a PZT film. To further improve write disturbance and nondestructive readout characteristics, better optimization on memory structure, ferroelectric properties, writing and reading pulse magnitudes, and bias timing of bitline, among others, would be required.

REFERENCES

[1] J. F. Scott and C. A. Paz de Arauzo, "Ferroelectric memories," *Science*, vol. 246, no. 4936, pp. 1400–1405, Dec. 1989.

[2] H. Ishiwara, "Current status and prospects of FET-type ferroelectric memories," *J. Semicond. Technol. Sci.*, vol. 1, no. 1, pp. 1–14, Mar. 2001.

[3] "International Technology Road Map for Semiconductors (ITRS)," pp. 8–10, 2005. [Online]. Available: http://www.itrs.net/Links/2005ITRS/ERD2005.pdf

[4] S.-M. Yoon and H. Ishiwara, "Memory operation of 1T2C-type ferroelectric memory cell with excellent data retention characteristics," *IEEE Trans. Electron Devices*, vol. 48, no. 9, pp. 2002–2008, Sep. 2001.

[5] S. B. Xiong and S. Sakai, "Memory properties of $SrBi_2Ta_2O_9$ thin film prepared on SiO_2/Si substrates," *Appl. Phys. Lett.*, vol. 75, no. 11, pp. 1613–1615, Sep. 1999.

[6] K.-H. Kim, J.-P. Han, S.-W. Jung, and T. P. Ma, "Ferroelectric DRAM (FEDRAM) FET with metal/$SrBi_2Ta_2O_9$/SiN/Si gate structure," *IEEE Electron Device Lett.*, vol. 23, no. 2, pp. 82–84, Feb. 2002.

[7] H. Saiki and E. Tokumitsu, "Ferroelectric split-gate-field-effect-transistors for nonvolatile memory cell array," *IEICE Trans. Electron.*, vol. 87, no. 10, pp. 1700–1705, Oct. 2004.

[8] T. P. Ma and J.-P. Han, "Why is nonvolatile ferroelectric memory field-effect transistor still elusive?" *IEEE Electron Device Lett.*, vol. 23, no. 7, pp. 386–388, Jul. 2002.

[9] C. T. Black, C. Farrell, and T. J. Licata, "Suppression of ferroelectric polarization by adjustable depolarization field," *Appl. Phys. Lett.*, vol. 71, no. 14, pp. 2041–2043, Oct. 1997.

[10] B. Park, S. Shouriki, E. Tokumitsu, and H. Ishiwara, "Fabrication of $PbZr_xTi_{1-x}O_3$ films on Si structures using Y_2O_3 buffer layers," *Jpn. J. Appl. Phys.*, vol. 37, no. 9B, pp. 5145–5149, Sep. 1998.

[11] T. Hirai, Y. Fujisaki, K. Nagashima, H. Koike, and Y. Tarui, "Preparation of $SrBi_2Ta_2O_9$ film at low temperatures and fabrication of a metal/ferroelectric/insulator/semiconductor field effect transistor using $Al/SrBi_2Ta_2O_9/CeO_2/Si$ (100) structures," *Jpn. J. Appl. Phys.*, vol. 36, no. 9B, pp. 5908–5911, Sep. 1997.

[12] S. Horita and T. D. Khoa, "Gate voltage reduction of a ferroelectric gate field effect transistor memory with an intermediate electrode on data-reading," *Jpn. J. Appl. Phys.*, vol. 42, no. 4A, pp. L365–L368, Apr. 2003.

[13] T. D. Khoa and S. Horita, "Retention and read endurance characteristics of a ferroelectric gate field-effect transistor memory with an intermediate electrode," *Jpn. J. Appl. Phys.*, vol. 43, no. 4B, pp. 2220–2225, Apr. 2004.

[14] T. D. Khoa and S. Horita, "Analysis on operation of a F-FET memory with an intermediate electrode," *IEEE Trans. Electron Devices*, vol. 51, no. 5, pp. 820–823, May 2004.

[15] B. N. Q. Trinh and S. Horita, "Operation of ferroelectric gate field-effect transistor memory with intermediate electrode using polycrystalline capacitor and metal–oxide–semiconductor field-effect transistor," *Jpn. J. Appl. Phys.*, vol. 45, no. 9B, pp. 7341–7344, Sep. 2006.

[16] S. Horita and B. N. Q. Trinh, "Nondestructive readout of ferroelectric-gate field-effect transistor memory with an intermediate electrode by using an improved operation method," *IEEE Trans. Electron Devices*, vol. 55, no. 11, pp. 3200–3207, Nov. 2008.

[17] A. K. Tagantsev, I. Stolichnov, N. Setter, J. S. Cross, and M. Tsukada, "Non-Kolmogorov–Avrami switching kinetics in ferroelectric thin films," *Phys. Rev. B, Condens. Matter*, vol. 66, no. 21, pp. 214 109-1–214 109-6, Dec. 2002.

[18] I. Stolichnov, A. Tagantsev, N. Setter, J. S. Cross, and M. Tsukada, "Crossover between nucleation-controlled kinetics and domain wall motion kinetics of polarization reversal in ferroelectric films," *Appl. Phys. Lett.*, vol. 83, no. 16, pp. 3362–3364, Oct. 2003.

[19] Y. W. So, D. J. Kim, T. W. Noh, J.-G. Yoon, and T. K. Song, "Polarization switching kinetics of epitaxial $Pb(Zr_{0.4}Ti_{0.6})O_3$ thin films," *Appl. Phys. Lett.*, vol. 86, no. 9, pp. 092 905-1–092 905-3, Feb. 2005.

[20] A. Gruverman, B. J. Rodriguez, C. Dehoff, J. D. Waldrep, A. I. Kingon, R. J. Nemanich, and J. S. Cross, "Direct studies of domain switching dynamics in thin film ferroelectric capacitors," *Appl. Phys. Lett.*, vol. 87, no. 8, pp. 082 902-1–082 902-3, Aug. 2005.

[21] W. J. Merz, "Domain formation and domain wall motions in ferroelectric $BaTiO_3$ single crystals," *Phys. Rev.*, vol. 95, no. 3, pp. 690–698, Aug. 1954.

[22] P. K. Larsen, G. L. M. Kampschöer, M. J. E. Ulenaers, G. A. C. M. Spierings, and R. Cuppens, "Nanosecond switching of thin ferroelectric films," *Appl. Phys. Lett.*, vol. 59, no. 5, pp. 611–613, Jul. 1991.

[23] J. F. Scott, *Ferroelectric Memories: Advanced Microelectronics*. Berlin, Germany: Springer-Verlag, 2000.

[24] A. Seike, K. Amanuma, S. Kobayashi, T. Tatsumi, H. Koike, and H. Hada, "Polarization reversal kinetics of a lead zirconate titanate thin-film capacitor for nonvolatile memory," *J. Appl. Phys.*, vol. 88, no. 6, pp. 3445–3447, Sep. 2000.

[25] S. Hayakawa, M. Kakumu, H. Takeuchi, K. Sato, T. Ohtani, T. Yoshida, T. Nakayama, S. Morita, M. Kinugawa, K. Maeguchi, K. Ochii, J. Matsunaga, A. Aono, K. Noguchi, and T. Asami, "A 1 μA retention 4Mb SRAM with a thin-film-transistor load cell," in *Proc. ISSCC Tech. Dig.*, Feb. 1990, pp. 128–129.

[26] S. Ikeda, S. Hashiba, I. Kuramoto, H. Katoh, S. Ariga, T. Yamanaka, T. Hashimoto, N. Hashimoto, and S. Meguro, "A polysilicon transistor technology for large capacity SRAMs," in *IEDM Tech. Dig.*, Dec. 1990, pp. 469–472.

[27] S. Ikeda, Y. Yoshida, S. Kamohara, K. Imato, K. Ishibashi, and K. Takahashi, "Threshold voltage-related soft error degradation in a TFT SRAM cell," *IEEE Trans. Electron Devices*, vol. 50, no. 2, pp. 391–396, Feb. 2003.

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