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Description	

Disturb-Free Writing Operation for Ferroelectric-Gate Field-Effect Transistor Memories With Intermediate Electrodes

Susumu Horita and Bui Nguyen Quoc Trinh

Abstract—To achieve disturb-free writing, we proposed a new writing operation for ferroelectric-gate field-effect transistor memories with intermediate electrodes. The writing voltages V_W applied to the wordlines for Pr^+ and Pr^0 memory states are the same pulse magnitudes, which consist of V_W^+ followed by V_W^- , whereas the bias timings of the bitline voltages differ from each other. The bitline voltage for the Pr^+ memory state is set high when V_W is set V_W^+ , and it is set to low by the time when V_W is changed to V_W^- . On the other hand, the bitline voltage for the Pr^0 memory state is set high until the whole writing pulse of $(V_W^+ + V_W^-)$ is finished. This is verified experimentally using a discrete circuit, which showed that the new writing operation achieves disturb-free writing. The memory consists of two transistors for data writing and reading. With the obtained experimental results, we discuss the possibilities of high integration of this memory as well as low reading voltage.

Index Terms—Disturb free, ferroelectric-gate memory, ferroelectric memory, nondestructive readout, write disturbance.

I. INTRODUCTION

FERROELECTRIC-GATE field-effect transistor (F-FET) memories are known to be one of the ultimate nonvolatile memories because of their remarkable features, such as nondestructive readout, high packing density, high reading speed, and low power consumption [1], [2], compared with ferroelectric random-access memories (FeRAMs). Furthermore, they have the advantages of low writing voltage, fast writing speed, and high endurance, compared with flash memories [3]. Although considerable researches on F-FET memories have been carried out [4]–[7], F-FET memories have not been commercialized because of problems such as short retention time [8], [9] and high writing voltage [10], [11]. To overcome these problems, we have proposed a new F-FET memory (denoted as IF-FET memory), in which an intermediate electrode (IE) for data writing is inserted between the ferroelectric capacitor C_f and the buffer layer (the gate) of a reading MOSFET (R-MOSFET) [13]–[15]. For data writing, using the IE, a writing voltage

V_W is applied directly to the C_f without voltage dropping on the buffer layer, and for data reading, a reading voltage V_R is applied between the top of C_f and the source of R-MOSFET with the IE being electrically floated. The memory needs another MOSFET for data writing in addition to R-MOSFET. The detailed configuration is given in Section II. Recently, we have also proposed an improved reading operation for perfect nondestructive readout [16]. In this operation, we used two kinds of memory states, a positive remanent-polarization Pr^+ state and a nearly nonpolarized Pr^0 state in C_f . For data reading, following a positive reading pulse with the magnitude V_R^+ to decode the memory state of C_f , a negative reading pulse with the magnitude V_R^- is applied to return the readout memory state to the initial one. It was confirmed experimentally that this reading operation improved the readout endurance more than 10^8 reading cycles and the retention time to exceed ten years [16], using a discrete circuit of IF-FET memory or one memory cell. It can be expected that the nondestructive readout by this operation endures until ferroelectric properties of C_f are degraded intrinsically such as fatigue and imprint. High endurance is another advantage of IF-FET over 1-transistor–1-capacitor (1T–1C) FeRAM in addition to the previously mentioned advantages of F-FET, except for that with high packing density. The high endurance results from the use of minor polarization-electric field (P – E) loops for data reading instead of full switching of polarization like that in FeRAM, which is explained in detail later. Ishiwaru *et al.* proposed a 1-transistor–2-capacitor (1T–2C), whose operation principle is similar to IF-FET, as a substitute of conventional F-FET. The total area of 2C in 1T–2C cannot be reduced to and overlapped with the gate area of R-MOSFET, which is not suitable for high integration of the memory. On the contrary, C_f of IF-FET can be fabricated just on the gate with the same area. The other comment on comparison with 1T–2C has been mentioned before [12].

However, disturbance of data in the writing operation (write disturbance) of IF-FET occurs in the case of memory array structure of an integrated circuit, which is a serious problem for practical use. We propose a new writing operation of IF-FET after demonstrating the problem related to a previous writing operation. By using a discrete circuit, we have also verified experimentally that the new writing operation is write disturb free as compared with the previous one. Finally, with the obtained results, we discuss the integration of IF-FET and the related issue of reading voltage.

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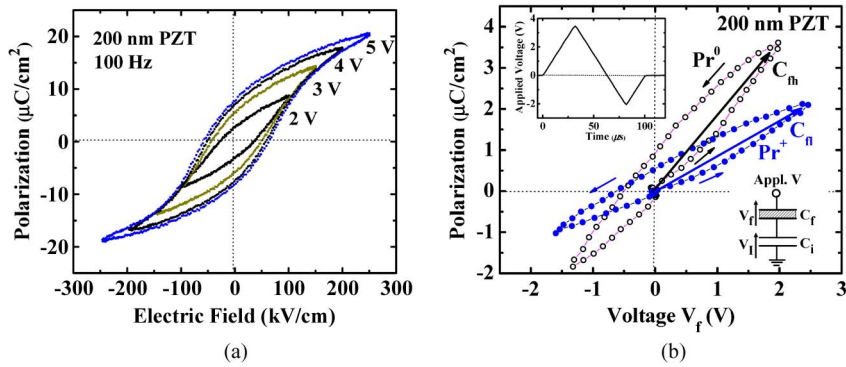


Fig. 5. (a) P - E hysteresis loops at 100 Hz of the PZT film used in this paper. (b) Relationships between the polarizations P and applied voltages V_f to the PZT film for Pr^+ and Pr^0 memory states in the similar condition of reading operation. The lower inset is the equivalent circuit of Fig. 1 at $V_D = 2.0$ V for this measurement. The upper inset shows the applied voltage V of a modified triangular waveform. From this, it can be seen that the C_{fh} is about twice as large as the C_{fl} .

top electrode)/ PtO_x /PZT/Pt/(RuO_x : bottom electrode) on an SiO_2/Si substrate. The ferroelectric layer was a 200-nm-thick and highly (100)/(001)-oriented PZT film, and the top electrode diameter D_t was 100 μm . The R-MOSFET was a commercial version of 2SK679A with $C_i = 180$ pF, V_D was 2 V, and R was 2 k Ω . The pulsewidths of V_W^+ , V_W^- , V_R^+ , and V_R^- were 50 μs , and the one period for data writing and data reading was 100 μs . Although it is not necessary for the writing period to be very long in the light of domain switching time and time constant of the measurement circuit, we allowed it to coincide with the reading one.

Fig. 5(a) shows the P - E hysteresis loops of the used PZT film, which were measured by a Sawyer-Tower circuit with a sine wave at 100 Hz. It can be observed that the P - E loops become saturated for applied voltages higher than 4 V. Thus, we set $V_W^+ = 4$ V, and the Pr^+ memory state had a positive remanent polarization near 4 V, as shown in Fig. 5(a). For clear readout by application of V_R^+ , the gate voltage of the R-MOSFET V_I for the Pr^+ memory state should be equal to or a little smaller than the threshold voltage of the MOSFET, $V_{th} = 1.4$ V. Therefore, we set V_R^+ to be 3.5 V, taking account of C_{fh} , C_{fl} , C_i , and V_{th} . The actual values of C_{fh} and C_{fl} are mentioned later. Application of V_W^- following V_W^+ for data writing is to produce a Pr^0 memory state from the Pr^+ state produced by V_W^+ . The polarization of the Pr^0 should be near the origin of the P - V hysteresis loop from two viewpoints of nondestructive readout and clear difference in output from the Pr^+ memory state. In addition, application of V_R^- has an important role to return any readout memory state to the initial memory state for the purpose of nondestructive readout. Because the optimum V_W^- and V_R^- depend on the properties of C_f and R-MOSFET and are related with each other, we determined them experimentally. Through the process mentioned as in the previous report [16], we set $V_W^+ = 4.0$ V, $V_W^- = -2.3$ V, $V_R^+ = 3.5$ V, and $V_R^- = -2.0$ V as the optimum pulse magnitudes in this paper.

Fig. 5(b) shows the relationships between the polarization P of the PZT film and the applied voltage V_f to the film for the Pr^+ and Pr^0 memory states. For this measurement, the circuit shown in Fig. 1 was used at $V_D = 2.0$ V, and the equivalent circuit is shown in the lower inset of Fig. 5(b). The applied

voltage was a modified triangular waveform as also shown in the upper inset of Fig. 5(b). The maximum and minimum voltages were 3.5 and -2.1 V, respectively; the duration times of the positive and negative voltages were 62.5 and 37.5 μs , respectively; and the total or one periodic time was 100 μs . The maximum and minimum voltages and the total time were matched with the actual reading conditions of V_R^+ , V_R^- , and one period, respectively. The duration times were unintentionally controlled because of the equipment specification, and their exact values are not physically important for this paper. The polarization P was calculated by the formula of $P = 4V_I \cdot C_i / (\pi D_t^2)$, and V_I was measured by an oscilloscope whose probe had the input resistance and capacitance of $R_p = 10$ M Ω and $C_p = 10$ pF, respectively. Because $C_i = 180$ pF was much larger than C_p and the time constant $R_p(C_i + C_p) = 1900$ μs was much larger than 100 μs , the input impedance of the oscilloscope can be ignored for this measurement. From this figure, it is shown that the curve slope of the Pr^+ state is lower than that of the Pr^0 state, and the capacitances of the PZT film for the Pr^+ and Pr^0 states are estimated to be ~ 70 and ~ 140 pF, respectively. It is also shown that both the P - V curves return to the measurement starting point or the origin after the one periodic measurement, which are similar to the minor loops shown in Fig. 1(b). This implies that nondestructive readout is possible in IF-FET.

To produce Pr^+ memory states by the new writing operation in a discrete circuit, we added another MOSFET (W_d -MOSFET) to the circuit of Fig. 1(a), as shown in the inset of Fig. 6(a). The source, gate, and drain of the W_d -MOSFET were connected with the ground, the top electrode of C_f , and the IE, respectively. When the pulse magnitude of the new writing voltage is a positive V_W^+ applied between the top electrode and the ground, the W_d -MOSFET is set to the ON-state so that a Pr^+ state is written into the C_f . When the pulse magnitude changes to a negative V_W^- , the W -MOSFET was set to the OFF-state so that the V_W^- was applied on the C_f and C_i in series. By this operation, the Pr^+ memory state written by V_W^+ remains because this writing operation is effectively equivalent to nondestructive readout operation. As a W_d -MOSFET, we used the same commercial MOSFET as the R-MOSFET. To write a Pr^0 memory state, the writing voltage was applied directly to the C_f

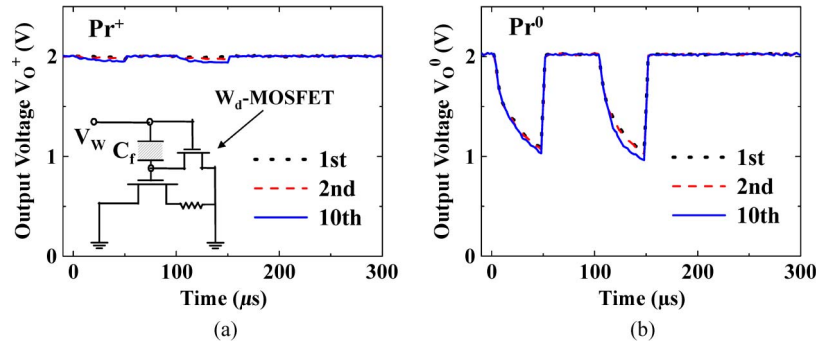


Fig. 6. Nondestructive readout characteristics for (a) the Pr^+ state and (b) the Pr^0 state, using the writing pulse magnitudes of $V_W^+ = 4.0$ V and $V_W^- = -2.3$ V, and the reading pulse magnitudes of $V_R^+ = 3.5$ V and $V_R^- = -2.0$ V. The numbers of readout times are the first, second, and tenth, where the retention or interval time is 1 min after each readout. The W_d -MOSFET was used only for writing Pr^+ memory state, which is not needed in integrated circuits.

without using W_d -MOSFET. After experimentally confirming the nondestructive readout of the memory states written by the new writing operation, we investigated the write-disturbance characteristics.

IV. RESULTS AND DISCUSSION

Fig. 6(a) and (b) shows the nondestructive readout characteristics for the Pr^+ and Pr^0 memory states, respectively. The memory state after each readout from the first to the tenth time was retained for 1 min under the condition that the IE was electrically floated and that the top electrode and the source and drain of the R-MOSFET were grounded. For every reading operation, the double periodic reading voltages were used. We can see that the characteristics for the Pr^0 state, as well as those for the Pr^+ state, show almost the same as any readout time. Then, the output difference ΔV_O constantly remains approximately 1 V through all of the readout times. However, V_O for the Pr^+ and Pr^0 states are decreased slightly with the readout times, and the V_O for the second reading pulses are always lower than the first ones for any readout time. We can speculate possible causes for this phenomenon as follows: The negative pulse magnitude V_R^- of the reading voltage was adjusted so that the memory state could return to the initial memory state from the readout state by V_R^+ . Because this adjustment was performed by only one readout time with one periodic reading voltage, the domain or polarization state of the C_f might not become steady state, compared with readout memory states subjected to more readout operations. Therefore, some amount of negative domains or upward domains might be increased a little from the initial memory state by repeating the readout operation. Because we obtained nondestructive readout endurance over 10^8 cycles as previously reported [16], it can be considered that the increment in volume of upward domain per one readout time is very small and is rapidly decreased with the number of readout times. Therefore, we can read out nondestructively the IF-FET memory written by the new writing operation. It is also noted that the response of V_O is slow to the V_R^+ pulse particularly in the Pr^0 state. This is not due to the circuit time constant (i.e., $(C_f/C_i) \cdot R$) because the time constant is approximately $0.2 \mu\text{s}$ and much smaller than the pulsewidth of $50 \mu\text{s}$. The main reason may be the requirement of some time to switch polarization domains, whose dynamics are governed by

nucleation and growth of the ferroelectric domain [17]–[20]. It has been reported that the volume fraction $\Delta P(t)/\Delta P(\infty) = p(t)$ of the switched domain, which is dependent of switching time t , can be described by $p(t) = 1 - \exp[-(t/t_0)^n]$. $\Delta P(t)$ is a switched polarization at t , and $\Delta P(\infty)$, which strongly depends on an electric field E_f in C_f , is a saturation of switched polarization at infinite time. t_0 and n are called the characteristics switching time and dimensionality, respectively, of the growing domains. It is well known that t_0 depends on E_f , crystal defect, grain size, electrode material, and so on. For example, Tagantsev *et al.* reported that $p(t)$ was approximately 80% at $t = 1$ ms for a 135-nm-thick (111)-textured PZT film with an IrO_x top electrode and $E_f = 100$ kV/cm [17]. In our case, E_f was approximately 100 kV/cm, and the switching time was approximately $50 \mu\text{s}$. Because V_I is proportional to $\Delta P(t)$, it varies with t corresponding to $p(t)$. Furthermore, by the transconductance g_m of the R-MOSFET and R , an infinitesimal intermediate voltage or gate voltage δV_I is amplified inversely to an infinitesimal output voltage $\delta V_O = -\delta V_I \cdot g_m \cdot R$. Therefore, it was observed that the response of V_O^0 for Pr^0 was fairly slow as shown in Fig. 6(b), compared with the V_R^+ square pulse. If E_f is increased by increasing V_R^+ , we can obtain much faster response because it has been reported that t_0 follows an experimental law of $t_0 \propto \exp(\alpha/E_f)$ [19], [21], where α is called as the activation field. Increasing V_R^+ , however, probably leads to higher power consumption. Because ferroelectric films have a high potential of domain switching time of a few nanoseconds [22]–[24], an operation time of IF-FET can be reduced to nanosecond order by improving the material properties of the ferroelectric film and electrode and the process techniques.

Fig. 7(a) shows the write-disturbance characteristics of Pr^0 memory state due to the previous writing operation. In this case, V_W for Pr^+ is 4.0 V, $V_W^+ = 4.0$ V, $V_W^- = -2.3$ V, $V_R^+ = 3.5$ V, and $V_R^- = -2.0$ V. From this figure, it can be seen that the output voltage V_O^0 for the Pr^0 write disturbance remains almost constant during the measurement, which means that there is no write disturbance, as expected. However, the V_O^0 for the Pr^+ writing disturbance quickly increases with the number of writing times. V_O^0 of the initial memory state before the Pr^+ write disturbance was approximately 0.9 V, which was almost equal to V_O^0 of the Pr^0 writing disturbance. This means that the memory state is destroyed and that severe write disturbance

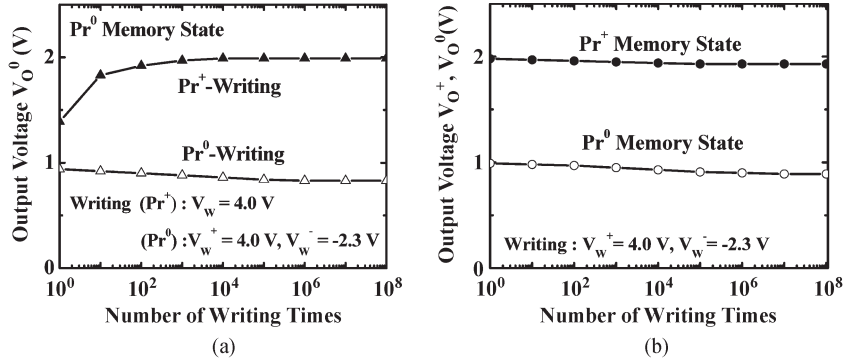


Fig. 7. (a) Write-disturbance characteristics of Pr^0 memory state due to the previous writing operation, in which the writing voltages for Pr^+ and Pr^0 states are different from each other. The Pr^+ write disturbance is severe, although the Pr^0 write disturbance is almost free. (b) Write-disturbance characteristics of Pr^+ and Pr^0 memory states due to the writing operation proposed in this paper, in which the writing voltages for both states are the same.

occurs. This is because the positive writing voltages V_W were applied continuously to the stored Pr^0 memory state, which was changed toward a positive polarization from nearly neutral. For the Pr^+ memory state, write disturbance due to both the Pr^+ and Pr^0 writing operations was not observed.

Fig. 7(b) shows that there were no write disturbances due to the new writing operation for both memory states. Strictly speaking, the V_O for both memory states are slightly decreased with the number of writing times. The same behavior is observed on V_O^0 due to the Pr^0 writing disturbance shown in Fig. 7(a). This is because the polarizations of both the memory states may gradually change from the initial states according to the number of writing times in the final steady state, as shown in Fig. 6. The variations are so small to be negligible for the memory operation, and there is room to improve them further by adjusting the ferroelectric property of C_f and the writing and reading pulse magnitudes [16]. Thus, from the results shown in Fig. 7(b), it can be said that the new writing operation is effective for write disturb free in IF-FET memory.

Finally, we discuss the integration issue of IF-FET. As previously mentioned, one ferroelectric capacitor (1C) of IF-FET can be formed directly on the gate oxide layer of R-MOSFET, the area of 1C being the same as that of the R-MOSFET gate. Under this condition of area, it is examined whether an operation voltage of IF-FET is reliable or not for commercialization. We estimate threshold reading voltages V_{TR}^+ for Pr^+ state and V_{TR}^- for Pr^0 state, at which V_I is equal to V_{th} of R-MOSFET. They are given by the following simple formulas [14]:

$$V_{TR}^+ = \left[\left(\frac{C_i}{C_{fh}} \right) + 1 \right] V_{th} \quad V_{TR}^- = \left[\left(\frac{C_i}{C_{fh}} \right) + 1 \right] V_{th}. \quad (1)$$

The assumptions for the estimation are as follows: The gate structure is metal/100-nm-thick ferroelectric/metal/3-nm-thick SiO_2 on Si in IF-FET, and V_{th} is 1.0 V. The relative dielectric constants of C_i , C_{fh} , and C_{fb} are 3.9, 200, and 400, respectively, according to the result shown in Fig. 5(b). Under this condition, we obtain $V_{TR}^+ = 1.65$ V and $V_{TR}^- = 1.33$ V. Because the difference between them is approximately 0.3 V, and the operation voltage can be less than 1.5 V, we can realize an IF-FET with the gate-stacked structure of metal/ferroelectric/metal/ SiO_2 . If a connection terminal of the IE is extended not from the edge of the source or drain but from the side in the channel width

direction, self-align process may be available at the expense of a small additional area. Thus, the actual area of IF-FET cell in integrated configuration is occupied roughly by 2T. We can reduce the occupied area if the 2T share the source or drain region in common. In static RAMs, thin-film transistors (TFTs) of polycrystalline Si are stacked over MOSFETs fabricated on a Si substrate to reduce the area per one memory cell [25]–[27]. If TFTs for W-MOSFETs are stacked over R-MOSFETs in integrated IF-FET, the packing density can be much increased. The drawback of IF-FET integration is technical complexity, such as fabrication of stacking TFTs over R-MOSFETs and the IEs between C_f and C_i , which induces high cost. This problem may be eased somewhat if the stacked layers (e.g., TFT) are fabricated at temperature lower than 400 °C. Low-temperature fabrication processes can reduce serious degradation of material properties (e.g., ferroelectric properties of C_f) in the under layers.

V. CONCLUSION

We have proposed a new operation for disturb-free writing in IF-FET memories. When Pr^+ and Pr^0 states are written into memory cells, wordlines are applied by the same writing voltages consisting of a positive pulse magnitude V_W^+ followed by a negative V_W^- , whereas the bitlines are applied by voltages that differ from each other. For the Pr^+ state, the bitline voltage falls down from high to low before the writing pulse magnitude changes from V_W^+ to V_W^- . On the other hand, for the Pr^0 state, the bitline voltage decreases when the whole writing voltage is finished. Because the waveform of the new writing voltage is similar to that of nondestructive reading voltage, IF-FET memory can be free from write disturbance. In fact, using the discrete circuit, we verified the usefulness of the new writing operation, showing disturb-free writing for any memory state for at least 10^8 writing times. Furthermore, we discussed the possibility of the high integration of IF-FET and estimated the reading voltage that would be sufficient for the commercialization of IF-FET using a PZT film. To further improve write disturbance and nondestructive readout characteristics, better optimization on memory structure, ferroelectric properties, writing and reading pulse magnitudes, and bias timing of bitline, among others, would be required.

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