Simultaneous Optimization of Skew and Control Step Assignments in RT-Datapath Synthesis

OBATA, Takayuki; KANEKO, Mineo

IEICE TRANSACTIONS on Fundamentals of Electronics, Communications and Computer Sciences, E91-A(12): 3585-3595

2008-12-01

Journal Article

http://hdl.handle.net/10119/8518

Copyright (C)2008 IEICE. Takayuki OBATA, Mineo KANEKO, IEICE TRANSACTIONS on Fundamentals of Electronics, Communications and Computer Sciences, E91-A(12), 2008, 3585-3595.

http://www.ieice.org/jpn/trans_online/
Simultaneous Optimization of Skew and Control Step Assignments in RT-Datapath Synthesis

Takayuki OBATA† and Mineo KANEKO†a), Members

SUMMARY As well as the schedule affects system performance, the control skew, i.e., the arrival time difference of control signals between registers, can be utilized for improving the system performance, enhancing robustness against delay variations, etc. The simultaneous optimization of the control step assignment and the control skew assignment is more powerful technique in improving performance. In this paper, firstly, we prove that, even if the execution sequence of operations which are assigned to the same resource is fixed, the simultaneous optimization problem under a fixed clock period is NP-hard. Secondly, we propose a heuristic algorithm for the simultaneous control step and skew optimization under given clock period, and we show how much the simultaneous optimization improves system performance. This paper is the first one that uses the intentional skew to shorten control steps under a specified clock period. The proposed algorithm has the potential to play a central role in various scenarios of skew-aware high level synthesis.

key words: high level synthesis, RT datapath, skew, wiring delay, scheduling

1. Introduction

In the logic level VLSI design, the clock skew is now utilized intentionally for improving system performances, enhancing the robustness against delay variations, reducing maximum peak power, etc., and significant efforts have been devoted to so-called clock-scheduling and simultaneous optimization of re-timing and clock-scheduling [1]–[6]. Recently, the importance and the impact of considering timing skew in the high level synthesis are recognized, and researches on skew-aware high level synthesis have started [7]–[11].

Because of the presence of several different approaches to the high level synthesis, the way of introducing intentional skew (intentionally controlled timing difference between the beginning of a control step and the working timing of each register and multiplexer) into high level synthesis is not unique. One possible scenario is that a conventional synthesis system incorporates intentional timing skew, and uses it to compensate the imbalance of function delays. One other possible scenario is that a concurrent datapath/floorplan synthesis system [12]–[19] incorporates intentional skew, and uses it to compensate imbalance of path delays (each path delay may include function delays and signal propagation delays). Similar to the clock schedule in the logic level design, the skew-aware high level design will contribute to reducing the clock period, and enhancing the robustness against delay variations. Furthermore, it will be demonstrated in this paper that the intentional skew will also contribute to reducing the number of control steps (makespan) for a target application.

It is well-known in the logic level design that the clock skew only is not enough for the highest performance, and the combination of the clock skew with the re-timing technique is a promising approach. Similar to this situation, in the skew-aware high level synthesis, the simultaneous optimization of the control step assignment and the skew assignment has a higher potential in performance optimization.

To discuss mathematically and logically the essential difference between skew and re-timing in a sequential circuit and our skew and control step assignment would be a hard task. The rather superficial difference between two are as follows.

1. Every register reads its input at every clock cycle in a sequential circuit. On the other hand, each register reads its input only scheduled clock cycle.
2. By re-timing technique in a sequential circuit, delay between registers will change, but still every register keeps to read its input at every clock cycle. On the other hand, in a datapath circuit, control step assignment (re-scheduling) does not change any delay between registers, but changes the timing in which each register reads its input.
3. Skew and re-timing for a sequential circuit target on reducing clock period. On the other hand, our skew and re-schedule can work not only for reducing clock period, but also for reducing schedule length. Furthermore, it is not clear which value (or concept) in a sequential circuit corresponds to the schedule length and varies by re-timing.

So, as a result, skew and re-timing algorithms designed so far for a sequential circuit can not be applied to our problem, especially for reducing schedule length.

Taking the peculiarity of the skew assignment into consideration, we assume that resource binding and the temporal order (not a specific control step assignment) of lifetimes of data assigned to the same register are fixed as a part of input description to our problem, and we try to optimize skew and control step assignments under those constraints. It is expected that, if we have a tool to solve this problem, it can be used also as a sub-tool for optimizing resource binding.

Manuscript revised June 24, 2008.
†The authors are with the School of Information Science, Japan Advanced Institute of Science and Technology, Nomi-shi, 923-1292 Japan.
a) E-mail: mkaneko@jaist.ac.jp
DOI: 10.1093/ietfjes/91-a.12.3585
Copyright © 2008 The Institute of Electronics, Information and Communication Engineers
and temporal order of lifetimes.

The first contribution of this paper is to show that our simultaneous control-step and skew optimization is an NP-hard problem, whereas the skew optimization under fixed control-step assignment and the constrained control-step optimization (that is, resource binding and the temporal order of lifetimes of data assigned to the same register are fixed) under fixed skew assignment are in the class P. The second contribution of this paper is a heuristic algorithm for our simultaneous control-step and skew optimization problem. In the past, the intentional skew was used mainly to shorten a clock period, and as a result, the clock period was not controlled intentionally. This paper is the first one that uses the intentional skew to shorten control steps under a specified clock period.

This paper is organized as follows. In Sect. 2, we summarize basic notations, and show motivational example. In Sect. 3, our simultaneous optimization of the control step assignment and the skew assignment is formulated. Section 4 deals with the computational complexity of our problem. We present a heuristic algorithm in Sect. 5. Experimental results are shown in Sect. 6. Finally, we present conclusions in Sect. 7.

2. Background and Motivation

2.1 Structural and Behavioral Descriptions of Datapath Circuit

We assume that the input algorithm of high-level synthesis is described as a data flow graph (DFG in short) \((\mathcal{O}, \mathcal{D})\) where a vertex set \(\mathcal{O}\) is the set of operations and an edge set \(\mathcal{D}\) indicates data dependencies between operations.

The input algorithm is transformed to the datapath circuit by determining resource assignment, that is, the functional unit assignment \(\rho : \mathcal{O} \rightarrow \mathcal{F}\) and the register assignment \(\xi : \mathcal{O} \setminus \mathcal{U} \rightarrow \mathcal{R}\), where \(\mathcal{F}\) is a set of functional units, \(\mathcal{R}\) is a set of registers, \(\mathcal{U}\) is a set of operations whose outputs are not written to registers, and \(\xi(o) = r\) means that the output data of the operation \(o\) is assigned to a register \(r\) (the output of \(o\) is written in \(r\)). Interconnections and multiplexers in the datapath part are so designed that, for each operation \(o_i\) with \((o_i, o_j) \in \mathcal{D}\), the input register \(\xi(o_i)\) is connected to the functional unit \(\rho(o_i)\) and \(\rho(o_j)\) is connected to the output register \(\xi(o_j)\). As an example, Fig. 1(b) shows the datapath circuit obtained from Fig. 1(a) with the resource assignment \(\rho(o1) = FU1, \rho(o2) = FU2, \rho(o3) = FU2, \rho(o4) = FU1, \rho(o5) = FU1, \xi(o1) = r2, \xi(o2) = r5, \xi(o3) = r3, \xi(o4) = r4, \xi(o5) = r1\).

The behavior of the datapath circuit, on the other hand, is determined by the arrival timing of control signals to registers and multiplexers. We let \(\mathcal{M}\) be the set of all registers (and multiplexers), and \(\mathcal{S}\) denotes the set of all control signals, where \(c^o_i \in \mathcal{S}\) represents the control signal which is related to the execution of \(o \in \mathcal{O}\) and is sent to \(x \in \mathcal{M}\). The arrival timing is partly determined by the control step assignment \(\sigma : \mathcal{S} \rightarrow \mathbb{Z}_+\), and the rest by the timing skew \(\tau : \mathcal{M} \rightarrow \mathbb{R}\). As the result, the control signal \(c^o_i\) reaches \(x\) at the time \(\sigma(c^o_i) \cdot \text{clk} + \tau(x)\), where \(\text{clk}\) is a clock period.

2.2 Motivational Example

Figure 2(a) shows an example of a DFG. We assume that the resource binding has been finished, and for each operation, signal path delays from an input register to an output register via a functional unit has been obtained. In general, data path from a multiple-bit register to a multiple-bit register must be

![Fig. 1 Example of DFG and RT-Level architecture.](image1)

![Fig. 2 Several different types of skew aware designs.](image2)
a multiple-input, multiple-output combinatorial circuit, and hence data path from a register to a register includes multiple signal paths having different delays. We will characterize each register-to-register data path with the maximum and the minimum among those delays, and we call them the maximum delay and the minimum delay, respectively. In Fig.2(a), the maximum and the minimum delays are indicated like 6/2 for $O_2$, 8/3 for $O_3$, etc. The assignment of data to registers is indicated as $r_i$ beside each arc.

Figure 2(b) shows a schedule of 6 control signals $c_{r_1}$, $c_{r_2}$, $c_{r_3}$, $c_{r_4}$, $c_{r_5}$, and $c_{r_6}$. The number written beside a slant solid (broken) arrow shows maximum (minimum) delay of the corresponding operation. The schedule requires 4 control steps, and its minimum clock period is 8 (the total computation time is $8 \times 4 = 32$). This is an optimum schedule under zero skew if the number of control steps is restricted to smaller than or equal to 4 (See Fig. 2(b)). When we assign skew ($\tau(r_1)$, $\tau(r_2)$, $\tau(r_3)$) = (0, 1, 1), the minimum clock period can be reduced to 7 (the total computation time is now $7 \times 4 + 1 = 29$). The situation is illustrated in Fig. 2(c). When we assign skew ($\tau(r_1)$, $\tau(r_2)$, $\tau(r_3)$) = (0, 6, 2) and we keep clock period to 8, we can modify the schedule and the number of control steps can be reduced to 3 (totally, $8 \times 3 + 2 = 26$). The situation is illustrated in Fig. 2(d). Figure 2(e) shows an optimum schedule and skew assignment. If we try to keep the number of control steps to 3, the minimum clock period is now 7 (totally, $7 \times 3 + 2 = 23$).

Skew is conventionally utilized only for reducing clock period (Fig. 2(c)). However, in many design flows, the clock period can not be determined freely upon convenience of a single datapath circuit. If we need to design a datapath under a given clock period, the conventional skew optimization can not be used directly. As it is shown by Design 3 in Fig. 2(d), the simultaneous optimization of the skew assignment and the control step assignment is necessary for datapath synthesis under a given clock period. Also in the case for minimizing the latency (Design 4 in Fig. 2(e)), the skew assignment and the control step assignment must be treated simultaneously.

3. Simultaneous Optimization of Control Step and Skew Assignments

3.1 Formulation of the Problem

Our simultaneous optimization problem, $(\sigma, \tau, clk)$-optimization, receives a data flow graph $G$, resource assignments $\rho$, $\xi$, and the execution order of operations assigned to the same FU, and the production order of data assigned to the same register (the function next introduced later reflects such information), and outputs $\sigma, \tau$ and $clk$.

Figure 3 illustrates the correct timing of control signals with respect to the execution of $o_j$. We assume that $o_j$ is an operation generating an input of $o_j$, and the output of the operation $o_j$ is written in a register $r_j$ ($\xi(o_j) = r_j$). On the other hand, the resource $x_i$ is either a register which stores the input data for $o_j$, an input multiplexer of a FU $p(o_j)$, or an input multiplexer of $r_j$. The “setup constraint” (the arrival of the control signal $c_m^{o_j}$ has to be later than the arrival of the result of $o_j$) is formulated as

$$\sigma(c_m^{o_j}) \cdot clk + \tau(x_i) + t_{err} + D_{n-x-r_j}^{o_j} + s \leq \sigma(r_j) \cdot clk + \tau(r_j) \quad (1)$$

where $o_j$ is either the operation that generates the input of $o_j$ stored in a register $x_i$ or $o_j$ in case $x_i$ is a multiplexer at the input of $p(o_j)$ or $r_j$. $D_{n-x-r_j}^{o_j}$ is the maximum path delay from $x_i$ to $r_j$ related to the execution of $o_j$. $t_{err}$ is a timing margin, and $s$ is the setup time of the register $r_j$.

On the other hand, the “hold constraint” (the arrival of $c_m^{o_j}$ has to be earlier than the destruction of the result of $o_j$) is given as

$$\sigma(r_j) \cdot clk + \tau(r_j) + t_{err} \leq \sigma(c_m^{next(x_i,o_j)}) \cdot clk + \tau(x_i) + d_{n-x-r_j}^{o_j} - h \quad (2)$$

where $d_{n-x-r_j}^{o_j}$ is the minimum path delay from $x_i$ to $r_j$ related to the execution of $o_j$, and $h$ is the hold time of $r_j$. $next(x_i,o_j)$ is the operation next to $o_j$ on the resource $x_i$. In case that several operations are chained, setup and hold constraints are formulated between input registers to the first operation, intermediate multiplexers located on the chaining path, and the output register of the last operation of the chain. Note that, when the control step assignment $\sigma$ is variable, we can set $0 \leq \tau(x) < clk$ for all $x \in M$ without loss of optimality.

Note that schedule and skew for an input multiplexer of a register is trivial. Let $m$ be an input multiplexer of a register $r$. For all operations $o$ which are assigned to the same register $r$, the maximum path delays $D_{m-o}^{r}$ have almost the same value, and also the minimum path delays $d_{m-o}^{r}$ have almost the same value. So we can set $\sigma(c_m^{o})$ and $\tau(m)$ as following:

$$\sigma(c_m^{o}) = \left[\frac{\sigma(c_m^{o}) \cdot clk + \tau(r) - D_{m-o}^{r}}{clk}\right],$$

$$\tau(m) = \tau(r) - D_{m-o}^{r} - \left[\frac{\tau(r) - D_{m-o}^{r}}{clk}\right] \cdot clk.$$
function of $|\mathcal{M}|$ and $CS$ (the number of control steps). Since $|\mathcal{M}|$ is fixed, $CS$ is our objective to be minimized in terms of circuit size. On the other hand, the computation time of a circuit can be evaluated with $clk \cdot CS$. Hence, we choose $clk \cdot CS + \lambda \cdot CS$ as the objective to be minimized, where $\lambda$ is a weighting coefficient.

Whether an instance has a feasible solution or not can be tested easily by relaxing integer-valued problem into real-valued problem, that is, by relaxing $\sigma : S \rightarrow \mathbb{Z}$ into $\sigma : S \rightarrow \mathbb{R}_{\geq 0}$. We will call $\sigma : S \rightarrow \mathbb{R}_{\geq 0}$ a real-valued schedule and it is computed by using a real-domain schedule constraint graph $G_{rs} = (S, E_{rs})$. The vertex set $S$ is the set of all control signals. The weighted edge set $E_{rs}$ corresponds to the following constraint inequalities obtained from (1)–(2) assuming variables $\tau$ equal to zero.

\[
\begin{align*}
\sigma(e_{r_i}^{o_i}) &\geq \sigma(e_{r_i}^{i_i}) + D_{r_i}^{r_j} + s + t_{err} \quad (3) \\
\sigma(e_{e_{r_i}}^{x_i}(x_{o_i})) &\geq \sigma(e_{x_{r_i}}^{y_i}) - d_{r_i}^{r_j} + h + t_{err} \quad (4)
\end{align*}
\]

That is, corresponding to (3)–(4), we add $(e_{r_i}^{o_i}, e_{r_i}^{i_i})$ with its weight $D_{r_i}^{r_j} + s + t_{err}$ and $(e_{x_{r_i}}^{y_i}, e_{x_{r_i}}^{x_{o_i}}(x_{o_i}))$ with its weight $-d_{r_i}^{r_j} + h + t_{err}$. The longest path length to each vertex from a source in $G_{rs}$ provides a feasible and optimal (in terms of $clk \times CS \rightarrow min$) real-valued schedule.

**Theorem 1.** If and only if there is no positive cycle in $G_{rs}$, there is a feasible assignment of $\sigma$ and $\tau$.

If there is no feasible real-valued schedule, there is no feasible assignment of $\sigma$ and $\tau$ because if there is a feasible assignment of $\sigma$ and $\tau$, we can compute the actual time of control signals in the form of $\sigma(e_{r_i}^{o_i}) \cdot clk + \tau(x_i)$. When $clk$ is sufficiently small, $\tau$ is also small, nearly equal to zero, and we can assume that $\sigma(e_{r_i}^{o_i}) \cdot clk$ takes an arbitrary real value. That is a reason why if there is a feasible real-valued schedule, there is a feasible assignment of $\sigma$ and $\tau$.

$\sigma$ takes an integer value and $\tau$ takes a real value, so if one of $clk$ and $CS$ is fixed, the problem becomes a Mixed Integer Linear Programming Problem. We show an optimization algorithm to compute optimum $\sigma$ and $\tau$ using MILP solver in Fig. 4. Although the algorithm computes an optimum solution, it takes impractical time.

**3.2 Partial Problems**

Because simultaneous optimization of $\sigma$, $\tau$, $clk$ is a hard problem, we consider partial problems. We assume that one of $\sigma$, $\tau$, $clk$ is fixed, and try to optimize the other two.

$(\sigma, clk)$-optimization is the problem to optimize $\tau$ and $clk$ while keeping control schedule $\sigma$ unchanged. Because $\tau$ and $clk$ take real values, $(\sigma, clk)$-optimization problem can be formulated as LP problem. An efficient graph theoretic approach has been proposed [9].

$(\sigma, clk)$-optimization is the problem to optimize $\sigma$ and $clk$ under given skew $\tau$. Conventional high level synthesis systems treat $(\sigma, clk)$-optimization with zero skew.

$(\sigma, \tau)$-optimization is the problem to optimize $\sigma$ and $\tau$ under a give clock period $clk$. In most cases $clk$ may be determined considering various factors, and we often encounter this type of optimization problem. $(\sigma, \tau)$-optimization is also a good candidate subroutine for solving the original $(\sigma, \tau, clk)$-optimization. That is, by repeating $(\sigma, \tau)$-optimization with a systematic sweep of $clk$, we can find a best solution for $(\sigma, \tau, clk)$-optimization. Thus, we discuss about $\sigma$ and $\tau$ optimization under given $clk$ in the rest of this paper.

**4. Computational Complexity of $(\sigma, \tau)$-Optimization Problem**

$(\sigma, \tau)$-optimization problem itself is an important problem which we will encounter in various design styles. It may also play an important role in solving the original $(\sigma, \tau, clk)$-optimization as a powerful subroutine.

The following theorem is one highlight of this paper.

**Theorem 2.** $(\sigma, \tau)$-optimization problem is NP-hard.

As it is mentioned in Sect. 3.1, our $(\sigma, \tau)$-optimization problem receives resource assignment and operation order on each FU as a part of input instance. It can be easily seen that, if the skew $\tau$ is fixed a priori (zero skew is one choice), $\sigma$-optimization problem with given resource assignment and given operation order on each FU is in class P. In contrast, even if resource assignment and operation order on each FU are specified, our $(\sigma, \tau)$-optimization is a NP-hard problem.

This result would be important in the sense that it shows us a broad and crucial guideline for designing a solution algorithm. That is, the result implies that there is no polynomial time algorithm for $(\sigma, \tau)$-optimization problem unless $P = NP$. It also suggests that we need to design a heuristic algorithm, otherwise we have to use an algorithm that is essentially the same with full search.

Based on this result, we will present a heuristic algorithm for $(\sigma, \tau)$-optimization in the next section. As it is the case for most NP-hard problems, the proof of NP-hardness do not have any direct relation to our heuristic algorithm.

Our proof of Theorem 2 is based on the polynomial time reduction from 3SAT to the decision version of $(\sigma, \tau)$-optimization problem. The detailed proof is presented in

![Fig. 4](image-url)
Appendix.

5. Heuristic Algorithm

In this section, we show a heuristic algorithm for this \((\sigma, \tau)\)-optimization problem.

5.1 Skew Constraint Graph

From (1) and (2), we have

\[
\tau_r - \tau_m \geq (\sigma^m_{\alpha} - \sigma^m_{\beta}) \cdot \text{clk} + \tau_{err} + D^m_{\text{m-r}} + s, \tag{5}
\]

\[
\tau_m - \tau_r \geq (\sigma^m_{\beta} - \sigma^m_{\alpha \text{next}(m,o)}) \cdot \text{clk} + \tau_{err} - d^m_{\text{m-r}} + h. \tag{6}
\]

We generate a skew constraint multigraph \(G_\tau = (V, E)\) from (5) and (6) as shown in Fig. 5. \(V\) is a set of multiplexers, registers and one auxiliary source node \(v_s\). A set of weighted edges \(E\) is the union of a set of edges reflecting (5) or (6) (i.e., an edge \((m, r)\) with its weight \((\sigma^m_{\alpha} - \sigma^m_{\beta}) \cdot \text{clk} + \tau_{err} + D^m_{\text{m-r}} + s\) or an edge \((r, m)\) with its weight \((\sigma^m_{\beta} - \sigma^m_{\alpha \text{next}(m,o)}) \cdot \text{clk} + \tau_{err} - d^m_{\text{m-r}} + h\) over all operations), and a set of auxiliary edges \(\{(m, v_s)|m \in V \setminus v_r\};\{v_s, m)|m \in V \setminus v_r\}\). Edge weights for \((m, v_r)|m \in V \setminus v_r\) and \((v_s, m)|m \in V \setminus v_r\) are \(-\text{clk}\) and 0, respectively. Then, skew assignment problem is now considered as the problem to assign real values to vertices in \(G_\tau\). Once \(\sigma\) is fixed, maximum path lengths from \(v_s\) to other vertices give us a solution, i.e., skews of registers and multiplexers. If \(G_\tau\) has a positive cycle, feasible skew schedule does not exist.

5.2 Schedule Constraint Graph

From (1) and (2) with regarding integral \(\sigma\), we have

\[
\sigma(c'_{r_j}) = \sigma(c''_{r_j})
\]

\[
\geq \left[ (\tau(x_i) - \tau(r_j) + \tau_{err} + D^r_{x_i-r_j} + s) / \text{clk} \right], \tag{7}
\]

\[
\sigma(c''_{r_j}) = \sigma(c''_{r_j})
\]

\[
\geq \left[ (\tau(r_j) - \tau(x_i) + \tau_{err} - d^r_{x_i-r_j} + h) / \text{clk} \right]. \tag{8}
\]

We generate a schedule constraint graph \(G_{\sigma} = (V_\sigma, E_\sigma)\).

\[
(\sigma^m_{\alpha} - \sigma^m_{\beta}) \cdot \text{clk} + \tau_{err} + D^m_{\text{m-r}} + s
\]

\[
(\sigma^m_{\beta} - \sigma^m_{\alpha \text{next}(m,o)}) \cdot \text{clk} + \tau_{err} + D^m_{\text{m-r}} + s
\]

\[
-\text{clk}
\]

\[
(\sigma^m_{\alpha} - \sigma^m_{\beta}) \cdot \text{clk} + \tau_{err} - d^m_{\text{m-r}} + h
\]

\[
(\sigma^m_{\beta} - \sigma^m_{\alpha \text{next}(m,o)}) \cdot \text{clk} + \tau_{err} - d^m_{\text{m-r}} + h
\]

\[
\text{Fig. 5} \: \text{Skew constraint multigraph.}
\]

\[
\text{Fig. 6} \: \text{We add an edge on a critical path in } G_\tau \text{ to } T.
\]

5.3 Heuristic Algorithm for \((\sigma, \tau)\)-Optimization Problem

Suppose we have computed \(\tau\) from \(G_\tau\), and consider the union \(T\) of a longest path from \(v_s\) to each node. Then, \(T\) is a spanning tree, and for each edge \((x_i, r_j)\) in \(T\), relative skew \((\tau(r_j) - \tau(x_i)) \mod \text{clk}\) is equal to either \((\tau_{err} + D^r_{x_i-r_j} + s) \mod \text{clk}\) or \((\tau_{err} - d^r_{x_i-r_j} + h) \mod \text{clk}\) depending on the edge weight. Therefore, we can consider the skew optimization problem as the problem to extract a spanning tree from \(G_\tau\). It is interesting that, once a spanning tree \(T\) of \(G_\tau\) is fixed, and tree edges are supposed to be critical path edges in \(G_\tau\), we can compute \(\tau\) from \(T \subset G_\tau\) without information of \(\sigma\). That is, for each edge \((x_i, r_j)\) in \(T\), we can put the relative-skew \((\tau(r_j) - \tau(x_i)) \mod \text{clk}\) as either \((\tau_{err} + D^r_{x_i-r_j} + s) \mod \text{clk}\) or \((\tau_{err} - d^r_{x_i-r_j} + h) \mod \text{clk}\) depending on the edge weight.

On the other hand in \(G_\sigma\), since the right hand side of (7), (8) has a ceiling, if the relative skew \((\tau(r_j) - \tau(x_i)) \mod \text{clk}\) is equal to \((\tau_{err} + D^r_{x_i-r_j} + s) \mod \text{clk}\) or \((\tau_{err} - d^r_{x_i-r_j} + h) \mod \text{clk}\), the edge weight reflecting inequality (7) or (8) is minimized. Therefore, to minimize \(CS\), it is efficient to set relative skew to \((\tau_{err} + D^r_{x_i-r_j} + s) \mod \text{clk}\) or \((\tau_{err} - d^r_{x_i-r_j} + h) \mod \text{clk}\) for as many edges as possible in a critical path. That is, we have to choose as many edges in a critical path in \(G_\sigma\) as edges of spanning tree in \(G_\tau\).

Our heuristic algorithm is shown in Fig. 7. We start with the spanning tree \(T\) whose edge set is \((v_s, m)|m \in V \setminus v_r\) assuming \(\tau(m) = 0\) for all \(m\). We replace \((v_s, m)\) with an edge corresponding to an edge on a critical path in \(G_\tau\) in one by one manner. In each time, we will test all candidate edges to be added to \(T\), and choose one edge which achieves smallest \(CS\).

In order to keep \(T\) being a tree, we use a partitioning to know which edge we can add and which edge we have to remove. Each connected component in \(T\)(\(\{v_s, x\}|x \in V\)) forms a partite set of a partition. Because \(T\) is a tree, only
Step 1. Generate $G_u$ and $G_v$.
Step 2. Generate an initial spanning tree $T \subset G_r$.
Step 3. Compute $\tau_T$ from $T$. Compute $\sigma$ from $G_u|_{v \in T}$. Let $\mathcal{P}$ be a critical path in $G_u|_{v \in T}$.
Step 5. For each edge $(u, v) \in G_r$ corresponding to $e \in \mathcal{P}$, try to generate $T_{(u,v)}$ from $T$ by adding $(u, v)$ and removing an appropriate edge. If we can compute $T_{(u,v)}$, compute skew assignment $\tau_{(u,v)}$ from $T_{(u,v)}$, and the number of control steps $CS_{(u,v)}$ from $G_u|_{v \in T}$.
Step 6. If $CS_{(u,v)} > CS$ or we cannot generate $T_{(u,v)}$ for all $(u, v)$ in Step 5, output $\tau_T$ and $\sigma$ and quit. Otherwise, set $T = T_{(u,v)}$ by such $(u, v)$ which achieves the smallest $CS_{(u,v)}$, and go to Step 3.

one edge from each partite set connects to $v_j$. If we generate $T_{(u,v)}$ by adding $(u, v)$ to $T$, we remove the edge between $v_j$ and the connected component to which $v$ belongs to. $G_r$ in Fig. 6 shows the replacement of edges. We add $(u, v)$ to $T$ only if $u$ and $v$ belong to different partite sets.

6. Experiments

The proposed heuristic algorithm for $(\sigma, \tau)$-optimization has been implemented using C programming language and tested on AMD Opteron $TM$ based PC. As input applications, we use three DAG algorithms modified from Jaumann wave filter, all-pole lattice filter and elliptic wave filter.

We have prepared 2 input instances for each input algorithm, each instance has different resource assignment, different operation order, and different delay assignment.

A path delay from an input register to an output register is the sum of delays of register-to-multiplexer, multiplexer-to-FU, FU, FU-to-multiplexer, and multiplexer-to-register. Maximum/minimum delays of multipliers and adders are 60/10 and 20/10, respectively. The other delays are given randomly. That is, minimum register-multiplexer and FU-multiplexer delays are chosen between 3 to 25, and the minimum multiplexer-register and multiplexer-FU delays are chosen from 2 to 15. The maximum delay of each path is set as 1.1 to 1.4 times larger value than its minimum delay.

Note that, for each input instance, those maximum delay values and minimum delay values, as well as resource assignment and operation order on each FU, are fixed throughout the experiments done with various different clock period $clk$. Of course, skew and control step are determined so that the setup condition and the hold condition are satisfied for all operations under the specified maximum delays, minimum delays, and clock period.

As the first experiment, for each instance, we have applied a schedule optimization without skew optimization (assuming zero skew) and the proposed algorithm.

Table 1 shows some of experimental results. The columns “#fu,” “#reg,” and “clk” represent the numbers of functional units, registers, and clock period of each instance, respectively. The column “CS” represents the number of control steps (makespan) of an output schedule and “time” represents the computation time in milli seconds.

Figures 8 through 10 show the experimental results graphically by plotting design points on the application time (i.e., $CS \times clk$) vs. clock period axes. Those plots are obtained by applying our algorithm repeatedly with increasing $clk$ by 1 at a time. Note again that, for each input instance, resource assignment, operation order on each FU, maximum delay values and minimum delay values are fixed, and these same values are used for different $clk$ values. Lower bound in each figure represents the minimum $CS \times clk$ of real-
valued schedule, which is introduced in Sect. 3.1. Since the solution space for real-valued schedule includes the one for integer-valued schedule (with skew), the smallest $CS \times clk$ achieved by real-valued schedule is no larger than the smallest $CS \times clk$ achieved by integer-valued schedule with skew.

As it is mentioned previously, conventional skew optimization algorithm is designed only for reducing the clock period. Even though its objective does not match with our objective; reduce the schedule length $CS$ under a given clock period, we will bravely compare our method with a two-step method; scheduling followed by skew optimization. Results are shown in Figs. 11 through 16. Design points given by “skew after schedule” are the result of the two-step algorithm; scheduling (with zero skew) followed by skew optimization. Figures 11, 12, and 13 compare our proposed algorithm with “skew after schedule.” On the other hand, “skew after proposed” is also a two-step algorithm; proposed algorithm followed by skew optimization for reducing clock period. Figures 14, 15, and 16 compare “skew after proposed” with “skew after schedule.”

From those experiments, advantage of our proposed method to the conventional skew optimization can be verified It is notable that the advantage is remarkable especially when we choose a large clock period (low clock frequency).

Finally, we briefly discuss area overhead and extra power consumption paid for skew control. The following discussion is based on logic synthesis results done by “Design Compiler (Version A-2007, 12-SP3)” with using library “class.” Table 2 shows the synthesis results of datapath components, and Table 3 shows the synthesis result of delay el-
Considering the maximum delay of an adder, we assume that the clock period is set to 7 ns. Then we need to prepare delay elements up to 7 ns. In case that the skew for each register or multiplexer is controlled by its own delay element, the area overhead for each register or multiplexer varies from 0 to around 20, and the extra power varies from 0 to around 3 μW. If we assume that skew values to registers and multiplexers spread equally from 0 to 7 ns, the average area overhead per register or multiplexer is around 10 which is around 6% of an 16 bit register and around 16% of an 16 bit 2-to-1 multiplexer. On the other hand, the average extra power per register or multiplexer is around 1.5 μW which is around 50% of an 16 bit register and around 130% of an 16 bit 2-to-1 multiplexer. In case that various clock skew values are generated from a single delay chain, the area overhead and extra power may possibly be decreased.

7. Conclusion

We have introduced a novel optimization problem, simultaneous schedule (control step assignment) and skew optimization problem. We presented a proof of NP-hardness and a heuristic algorithm for the simultaneous control step and skew optimization under given clock period. The algorithm has the potential to play a central role in various scenarios of skew-aware RT level synthesis. A study of the relation between the simultaneous optimization of skew and

![Fig. 14](image1.png)

**Fig. 14** Application time ($CS \times clk$) vs. $clk$ for Jaumann.

![Fig. 15](image2.png)

**Fig. 15** Application time ($CS \times clk$) vs. $clk$ for Lattice.

![Fig. 16](image3.png)

**Fig. 16** Application time ($CS \times clk$) vs. $clk$ for Elliptic.

<table>
<thead>
<tr>
<th>Table 2 Datapath components.</th>
</tr>
</thead>
<tbody>
<tr>
<td>16 bit adder</td>
</tr>
<tr>
<td>Max. delay [ns]</td>
</tr>
<tr>
<td>Min. delay [ns]</td>
</tr>
<tr>
<td>Area</td>
</tr>
<tr>
<td>Power [μW]</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Table 3 Delay element.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rising Delay [ns]</td>
</tr>
<tr>
<td>0.38</td>
</tr>
<tr>
<td>0.67</td>
</tr>
<tr>
<td>1.45</td>
</tr>
<tr>
<td>1.79</td>
</tr>
<tr>
<td>2.18</td>
</tr>
<tr>
<td>2.94</td>
</tr>
<tr>
<td>3.49</td>
</tr>
<tr>
<td>3.69</td>
</tr>
<tr>
<td>4.44</td>
</tr>
<tr>
<td>4.97</td>
</tr>
<tr>
<td>5.38</td>
</tr>
<tr>
<td>5.92</td>
</tr>
<tr>
<td>6.36</td>
</tr>
<tr>
<td>6.89</td>
</tr>
<tr>
<td>7.46</td>
</tr>
<tr>
<td>7.94</td>
</tr>
<tr>
<td>8.41</td>
</tr>
<tr>
<td>8.94</td>
</tr>
<tr>
<td>9.44</td>
</tr>
<tr>
<td>9.92</td>
</tr>
<tr>
<td>10.40</td>
</tr>
</tbody>
</table>
Acknowledgement

The authors would like to thank anonymous reviewers for their comments and suggestions which improved the presentation of this paper. The authors also would like to thank Dr. Iwagaki, JAIST, for his helpful supports on experiments. This work is partly supported by the Society for the Promotion of Science, Japan, under Grant-in-Aid for Scientific Research (C), No. 19560340, 2007–2008.

References


Appendix: Proof of NP-Hardness of (σ, τ)-Optimization Problem

We show the detailed proof of NP-hardness of (σ, τ)-Optimization Problem (Theorem 2).

Our proof is based on the polynomial time reduction from 3SAT to the decision version of (σ, τ)-optimization problem (In the following, we call it (σ, τ)-decision problem in short.).

First, we define the transformation from an instance of 3SAT problem to an instance of the (σ, τ)-decision problem. Let \((X, C)\) be an instance of 3SAT problem, where \(X = \{x_1, x_2, \cdots, x_n\}\) is a set of variables, \(C = c_1 \land c_2 \land \cdots \land c_m\) is a formula, and for each clause \(c_i = (l_{i_1} \lor l_{i_2} \lor l_{i_3})\), literal \(l_{ij}\) is either \(x_\ell\) or \(\neg x_\ell\) for some \(k\). An input instance of the decision version of (σ, τ)-optimization problem is a 8-tuple \((G, \rho, \xi, next, D, d, clk, CS_{spec})\), and the problem asks “Are there any feasible \(\sigma\) and \(\tau\) satisfying that the maximum control step is less than or equal to \(CS_{spec}\)?”

Data Flow Graph \(G = (O, D)\):

The set of vertices \(O\) is;

\[ O = \{O_{i\ell} | 0 \leq i \leq m\} \]

\[ \cup \{O_{ij} | 1 \leq i \leq m, 1 \leq j \leq 3\}\]

and the set of edges \(D\) is;

\[ D = \{\{(O_{i\ell}, O_{ij}) | i \leq i \leq m\} \]

\[ \cup \{\{(O_{ij}, O_{ij}), (O_{ij}, O_{ij}), (O_{ij}, O_{ij})\} | 1 \leq i \leq m\}\]

Please refer to Fig. A-1.

Resource assignments \(\rho\) and \(\xi\):

For operations, they are assigned to separate FUs (no FU sharing occurs). For data, we prepare \(n + 1\) registers named \(x_1, x_2, \cdots, x_n, y\), and we assign \(\xi(O_{ij}) = \xi(O_{ij}) = \cdots = \xi(O_{ij}) = y\), and \(\xi(O_{ij}) = x_\ell\), where the literal \(l_{ij}\) is either \(x_\ell\) or \(\neg x_\ell\), for all \(i\) and \(j\).

\[ next \]

Trivial from the data dependency specified by \(G = (O, D)\).

Maximum path delay \(D\) and minimum path delay \(d\):

Maximum path delays are set depending on the number

![Fig. A-1](image-url) A DFG for a 3SAT instance.
of negated variables in a clause.

1. For a clause $c_i = (x_j \lor x_k \lor \neg x_l)$; $D^{O_i}_{y-x_l} = D^{O_i}_{y-x_k} = D^{O_i}_{y-x_j} = D^{O_i}_{x_j-x_l} = 0.5, D^{O_i}_{x_j-x_k} = 3$.

2. For a clause $c_i = (x_j \lor x_k \lor \neg x_l)$; $D^{O_i}_{y-x_l} = D^{O_i}_{y-x_k} = 0.5, D^{O_i}_{y-x_j} = D^{O_i}_{x_j-x_l} = 1, D^{O_i}_{x_j-x_k} = 4$.

3. For a clause $c_i = (x_j \lor x_k \lor \neg x_l)$; $D^{O_i}_{y-x_l} = D^{O_i}_{y-x_k} = 0.5, D^{O_i}_{y-x_j} = D^{O_i}_{x_j-x_l} = 1, D^{O_i}_{x_j-x_k} = 4$.

4. For a clause $c_i = (\neg x_j \lor x_k \lor \neg x_l)$; $D^{O_i}_{y-x_l} = D^{O_i}_{y-x_k} = 1, D^{O_i}_{y-x_j} = D^{O_i}_{x_j-x_l} = 3, D^{O_i}_{x_j-x_k} = 4$.

On the other hand, we can assign an arbitrary value (between 0 and the corresponding maximum path delay) to the minimum path delay $d^{y}_{x-y}$, i.e., $0 < d^{y}_{x-y} \leq D^{y}_{x-y}$.

We set $clk = 1$.

**CS spec**: We set $CS_{spec} = 3m_0 + 4(m - m_0)$, where $m$ is the total number of clauses and $m_0$ is the number of clauses including only non-negated variables.

**Others**: We set $s, h, t_{err}$ to 0, for the simplicity purpose. Discussions do not lose the generality by this simplification, because we can generate an equivalent problem instance with non-zero $s, h, t_{err}$ by simply arranging the maximum path delay $D^{y}_{x-y}$ to $D^{y}_{x-y} - t_{err} - s$ and the minimum path delay $d^{y}_{x-y}$ to $d^{y}_{x-y} + t_{err} + h$. Based on this observation, the following discussions are made under $s = h = t_{err} = 0$.

The basic idea behind this transformation is to simulate the [0, 1] assignment to variables in 3SAT problem by the skew assignment to registers $x_1, x_2, \cdots, x_n$ in the $(\sigma, \tau)$-decision problem.

The first lemma ensures that the optimum solution for a problem instance obtained by the above transformation from an instance of 3SAT problem can be determined without depending on the minimum path delay information, and we need to care only maximum path delays.

**Lemma 1.** Let $o$ and $o'$ be distinct operations and there exist an edge $(o', o)$ in $G$. If there exist a directed path from $o$ to $next(\xi(o'), o')$ in $G$, the minimum path delay $d^{\xi(o')-\xi(o)}_{\xi(o')}$ does not affect $\sigma(\xi(o'))$.

**Proof.** If there exist a directed path from $o'$ to $next(\xi(o'), o')$ in $G$, we can sum up the set constraints of registers along this path, and we have

$$\sigma(\xi(o')) \cdot clk + \tau(\xi(o')) \leq \sigma(\xi(next(\xi(o')))) \cdot clk + \tau(\xi(o'))$$

It means that the hold constraint

$$\sigma(\xi(o')) \cdot clk + \tau(\xi(o'))$$

$$\leq \sigma(\xi(next(\xi(o')))) \cdot clk + \tau(\xi(o')) + d^{\xi(next(\xi(o')))-\xi(o)}$$

is satisfied automatically without depending on the value of $d^{\xi(o')-\xi(o)}$.

Next, we will introduce the following lemma which allows us to restrict the skew value to doubleton [0, 0.5·clk]. By this restriction, we can ensure the correspondence between [0, 1] assignment in 3SAT and the [0, 0.5·clk]-skew assignment in the $(\sigma, \tau)$-decision problem.

**Lemma 2.** If the clock period is $clk$ and each of maximum and minimum path delays has the value either $k \cdot clk$ or $(k + 0.5)clk$ for some integer $k$, there always exists a $(\sigma, \tau)$-optimum solution with only 0, 0.5clk skew values. (From an arbitrary $(\sigma, \tau)$-optimum solution, we can construct a $(\sigma, \tau)$-optimum solution having only 0, 0.5clk skew values. The time complexity of this transformation is $O(\mathcal{M})$.)

**Proof.** Let $\sigma$ and $\tau$ be an optimum solution of the $(\sigma, \tau)$-optimization for an input instance in which every path delay has the form either $k \cdot clk$ or $(k + 0.5)clk$ for some integer $k$. Let $\tau^*$ be the transformed version of $\tau$, which is obtained as follows.

$$\tau^*(x) = \begin{cases} 0 & \text{if } 0 \leq \tau(x) < 0.5clk \\ 0.5clk & \text{if } 0.5clk \leq \tau(x) < clk \end{cases}$$

Note that $\tau(x) \geq \tau^*(x)$ for all $x$. It will be proven that $\sigma$ and $\tau^*$ is also an optimum solution for the given instance. Since $\sigma$ is unchanged, it is enough to verify that the pair of $\sigma$ and $\tau^*$ is a feasible solution. For the setup constraint of any part

$$\sigma(\xi(o')) \cdot clk + \tau(\xi(o')) \geq \sigma(\xi(next(\xi(o')))) \cdot clk + \tau(\xi(next(\xi(o')))) + D^{\xi(next(\xi(o')))-\xi(o')},$$

we have

$$\sigma(\xi(o')) \cdot clk + \tau(x) + (\tau(x) - \tau^*(x)) \geq \sigma(\xi(next(\xi(o')))) \cdot clk + \tau(x) + D^{\xi(next(\xi(o')))-\xi(o')}$$

Since $\sigma(\xi(o')) \cdot clk$, $\tau(x)$, $\sigma(\xi(next(\xi(o')))) \cdot clk$, $\tau(x)$ and $D^{\xi(next(\xi(o')))-\xi(o')}$ are all multiples of 0.5clk, and $D^{\xi(next(\xi(o')))-\xi(o')}$ is less than or equal to $3m_0 + 4(m - m_0)$, we can truncate $(\tau(x) - \tau(x)) - (\tau(x) - \tau^*(x))$ to 0, and we have

$$\sigma(\xi(o')) \cdot clk + \tau^*(x) \geq \sigma(\xi(next(\xi(o')))) \cdot clk + \tau^*(\xi(x)) + D^{\xi(next(\xi(o')))-\xi(o')}$$

We can verify hold constraints for $\sigma$ and $\tau^*$ in a similar way, and we can conclude the feasibility of the pair $\sigma$ and $\tau^*$. □

From Lemmas 2 and 1, we can discuss an optimum solution for the problem instance obtained by the transformation from 3SAT only considering maximum path delays and doubleton [0, 0.5] for skew values.

**Proof of Theorem 1:** It is clear that the $(\sigma, \tau)$-decision problem is in the class NP.

The transformation from an instance of 3SAT ($(X, C)$) to an instance of the $(\sigma, \tau)$-decision problem ($(G, \rho, \xi, next, D, clk, CS_{spec})$) can be done in polynomial time. We claim that $(G, \rho, \xi, next, D, clk)$ has $\sigma$ and $\tau$ such that $\sigma_{\rho} - \sigma_{\rho'}$ is less than or equal to $3m_0 + 4(m - m_0)$ if and only if $(X, C)$ is satisfiable. It can be easily verified that $\sigma_{\rho} - \sigma_{\rho'}$ equals to $3m_0 + 4(m - m_0)$ if and only if
is satisfied for all $i, 1 \leq i \leq m$. For a clause $c_i = (x_j \lor x_k \lor x_l)$ (all non-negated variables), $\sigma(c_i^{O_i}) - \sigma(c_i^{O_{i-1}}) = 3$ if and only if at least one from $\tau(x_j), \tau(x_k)$ and $\tau(x_l)$ equals to 0.5 (See Fig. A-2), which corresponds to the fact that at least one from $x_j, x_k$ and $x_l$ is assigned 1 and the clause $c_i$ is satisfied. The similar arguments are satisfied for the other types of clauses (Fig. A-3 shows one other case where the clause includes exactly one negated variable). So, we can conclude that $\sigma(c_i^{O_m}) - \sigma(c_i^{O_0})$ equals to $3m_0 + 4(m - m_0)$ if and only if all clauses are satisfied. \hfill $\square$

Takayuki Obata received his B.E. degree in electrical and electronics engineering from Tokyo Institute of Technology, Tokyo, Japan, in 2001, and M.S. degree in information science from Japan Advanced Institute of Science and Technology, Ishikawa, Japan, in 2003. He is currently working toward his Ph.D. degree at Japan Advanced Institute of Science and Technology. His main research interest is high-level synthesis.

Mineo Kaneko received Bachelor of Engineering, Master of Engineering, and Doctor of Engineering degrees in electrical and electronic engineering from Tokyo Institute of Technology in 1981, 1983, and 1986, respectively. From 1986 to 1996, he worked at Tokyo Institute of Technology as a research associate, a lecturer, and an associate professor. In 1996, he transferred to Japan Advanced Institute of Science and Technology (JAIST), and currently he is a professor in the Graduate School of Information Science, JAIST. His research interests include circuit theory, CAD for VL-SIs, and signal processing. He is a member of IEEE and ACM.