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On Negation-Limited Circuit Complexity

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ABSTRACT

On Negation-Limited Circuit Complexity

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A central problem of the theory of computing is to understand the inherent complexity of computational tasks in terms of resources required. We study the complexity of Boolean functions over *circuit* model. While proving a superlinear lower bound on general circuits remain a hard open problem, we investigate a restricted version of circuits, called *negation-limited circuits*.

In this thesis, we first consider the negation-limited circuits over basis $\{\wedge, \vee, \neg\}$. We show some properties of negation-limited circuits. From such properties, we show lower bounds on size and depth of negation-limited circuits computing Boolean functions. In particular, we obtain a $5.33n$ lower bound on size of negation-limited circuits computing the parity functions. Then, we deal with the complexity of the negation-limited inverters. By the negation-limited inverters, the complexity of the general circuits is related to that of the negation-limited circuits. Thus, it is important to understand the negation-limited inverters. We show an upper bound on depth of negation-limited inverters. We also show a $7.33n$ lower bound on size. Under a natural assumption, we obtain an $\Omega(n \log n)$ lower bound on size for negation-limited inverters, while the best upper bound on size is $O(n \log n)$.

Next, we consider the negation-limited threshold circuits. We first show a lower bound on the minimum number of negation gates in threshold circuits computing any given Boolean function. We also show an upper bound on the minimum number of negation gates in threshold circuits computing some given Boolean functions which matches the lower bound.

For the inverters and the parity functions, we show the negation-limited threshold circuits computing such functions which contain minimum number of negation gates. As

an application of negation-limited circuit complexity, we obtain a lower bound on size of general threshold circuits computing any given Boolean function. In particular, such lower bounds for the parity functions match our upper bounds.

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Chapter 1

Introduction

A central problem of the theory of computing is to understand the inherent complexity of computational tasks in terms of resources required. We study the complexity of Boolean functions over *circuit* model. The circuit complexity is related to the complexity over many other important models of computations. For example, the size (the number of gates) of circuits is related to the time complexity of Turing machines, and the depth (the parallel computation time) of circuits is related to the space complexity of Turing machines [20]. In this thesis, we consider two types of circuits, *circuits over basis* $\{ \wedge, \vee, \neg \}$ and *threshold circuits*.

Shannon's counting argument [15] shows that for almost all Boolean function f of n variables the size of any circuit computing f is at least exponential in n. However, the best lower bounds for explicitly defined Boolean functions of n variables are quite small. For circuits over basis $\{ \wedge, \vee, \neg \}$, the largest known lower bound on the size of circuits is linear in n. For threshold circuits, superpolynomial lower bound on the size is shown only for depth 2 threshold circuits [8].

A restricted version of circuits called *monotone circuits*, has much success in proving lower bounds. *Monotone circuits* are circuits without *negation*, i.e., the number of negation is limited to 0. Exponential lower bounds on the size of monotone circuits over basis $\{ \wedge, \vee, \neg \}$ (i.e., circuits over basis $\{ \wedge, \vee \}$), for many explicitly defined Boolean functions are known [13, 3, 12]. Yao [22] showed that the class of Boolean functions computable by polynomial-size monotone threshold circuits of depth D form a proper hierarchy in

parameter D. That is, superpolynomial lower bounds on the size of depth D monotone threshold circuits are shown for all constant D. A natural intermediate step is the study of circuits with limited number of *negations*, i.e., *the negation-limited circuits*.

The complexity of negation-limited circuits has been investigated by many researchers [11, 7, 6, 14, 18, 4]. Markov [11] gives an explicit formula for the minimum number of negations required for circuits computing an arbitrary Boolean function. Santha and Wilson [14] have studied the number of negations required for small (e.g., constant) depth threshold circuits. The complexity of the negation-limited circuits and that of the general circuit are related by Fischer [6]. He showed that limiting the number of negations to $\lceil \log(n+1) \rceil$ in circuits computing an arbitrary Boolean function of n variables only causes a polynomial blowup in the circuit size.

In this thesis, we consider the complexity on circuits over $\{ \wedge, \vee, \neg \}$ and threshold circuits with limited number of negations. The remainder of this thesis is divided into 5 chapters. In Chapter 2, we describe elementary definitions and notations of Boolean functions and circuits.

In Chapter 3, we consider complexity of negation-limited circuits over basis $\{ \wedge, \vee, \neg \}$. We show some properties of negation-limited circuits. From such properties, we obtain lower bounds on the depth and the size of negation-limited circuits. In particular, we obtain a $5.33n$ lower bound on size of negation-limited circuits computing parity functions. We also show upper bounds on depth and size of negation-limited circuits computing Boolean symmetric functions.

In Chapter 4, we consider the complexity of the negation-limited inverters. We first show an upper bound on depth of negation-limited inverters, which seems to match the lower bound shown by Tanaka and Nishino [18]. Then, we show a $7.33n$ lower bound on size of negation-limited inverters. However, the best upper bound on size of negation-limited inverters is $O(n \log n)$ which is showed by Beals, Nishino and Tanaka [4], and it is conjectured that the minimum size of negation-limited inverters is $\Omega(n \log n)$. In this situation, we show an $\Omega(n \log n)$ lower bound on size of negation-limited inverters under a natural assumption.

In Chapter 5 and 6, we consider the negation-limited threshold circuits. We discuss the minimum number of negations in threshold circuits computing an arbitrary Boolean function in Chapter 5. We show that the lower bound which shown by Santha and Wilson [14] can be slightly improved. Then, we show an upper bound on the minimum number of negations in threshold circuits computing some Boolean functions which matches the lower bounds, i.e., our lower bound is *tight*.

However, our lower bound is not tight for all Boolean functions. In Chapter 6, we show that the lower bound of minimum number of negations can be improved for all *single-output* Boolean functions and some *multi-output* Boolean functions. The minimum size of negation-limited threshold circuits computing inverters and parity functions with respect to depth are shown. As an application of negation-limited circuit complexity, we obtain a lower bound on size of general threshold circuits (i.e., threshold circuits without restriction on negations) computing an arbitrary Boolean function. In particular, such a lower bound for parity functions matches our upper bound. This result completely answers an open problem posed by Wegener [21].

Chapter 2

Preliminaries

2.1 Boolean functions

Let $x = (x_1, \ldots, x_n)$ be a *vector of n Boolean variables* $x_1, \ldots, x_n$. By $\|x\|$ we denote the number of 1's in Boolean vector $x \in \{0,1\}^n$, i.e.,

$$\|x\| = \|(x_1, \ldots, x_n)\| = \sum_{i=1}^{n} x_i \,.$$

A *(single-output) Boolean function of n variables* is any mapping f from $\{0,1\}^n$ to $\{0,1\}$. A *collection of m (≥ 1) Boolean functions of n variables* (i.e., an m-output Boolean function) is a vector $F = (f_1, \ldots, f_m)$ of Boolean functions $f_1, \ldots, f_m$ of n variables. A Boolean function is a collection of *one* Boolean function.

2.1.1 Decreases and increases of Boolean functions

A chain $\alpha = (\alpha^0, \ldots, \alpha^n)$ is a vector of vectors $\alpha^l \in \{0,1\}^n$ such that $\|\alpha^l\| = l$ and $\alpha^l \leq \alpha^{l+1}$, i.e.,

$$\alpha_i^l \leq \alpha_i^{l+1} \quad \text{for each} \quad 1 \leq i \leq n \,.$$

For a Boolean function f and a chain α, let $S(f,\alpha) \subseteq \{\, 0, \ldots, n \,\}$ be *the satisfying set of f over chain α* such that

$$l \in S(f,\alpha) \quad \text{if} \quad f(\alpha^l) = 1 \,.$$

A satisfying set $S(f,\alpha)$ can be represented as following form: For some $0 \leq k \leq \lceil n/2 \rceil$ and $0 \leq l_1 < l_2 < \cdots < l_{2k-1} < l_{2k} \leq n+1$

$$S(f,\alpha) = [l_1, l_2) \cup \cdots \cup [l_{2k-1}, l_{2k}) \,,$$

where $[a,b) = \{\, a, a+1, \ldots, b-1 \,\}$ for integers $a \leq b$.

An index $l \in \{\, 1, \ldots, n \,\}$ is a *decrease of f over chain α* if $l-1 \in S(f,\alpha)$ and $l \notin S(f,\alpha)$, i.e., $f(\alpha^{l-1}) > f(\alpha^l)$. Similarly, an index $l \in \{\, 1, \ldots, n \,\}$ is an *increase of f over chain α* if $l-1 \notin S(f,\alpha)$ and $l \in S(f,\alpha)$, i.e., $f(\alpha^{l-1}) < f(\alpha^l)$. For a collection of Boolean functions $F = (f_1, \ldots, f_m)$, an index l is a *decrease of F over chain α* if l is a decrease of f_j over chain α for some $1 \leq j \leq m$. An index $l \in \{\, 1, \ldots, n \,\}$ is a *increase of F over chain α* if l is an increase of f_j over chain α for some $1 \leq j \leq m$.

By $dec(F,\alpha)$ and $inc(F,\alpha)$, we respectively denote the *set of decreases of F* and the *set of increases of F over chain α*. By $d(F)$ we denote the *maximum $|dec(F,\alpha)|$ over all chains α*. A collection of Boolean functions F is called *monotone* if $d(F) = 0$.

2.2 Circuits

A basis of circuits is a set of operations (i.e., Boolean functions) which are available. A *circuit* is a directed acyclic graph composed of nodes called *inputs* and *gates*. *Inputs* are nodes of in-degree 0 and labeled by elements of the set $\{0, 1, x_1, \ldots, x_n\}$. *Gates* are nodes of in-degree ≥ 1 and labeled by operations from the given basis, such that a gate of in-degree m is labeled by an operation of m variables. Some gates are designated the *output gates*.

The computation of a circuit is proceeded as follows. By Υ_G we denote the Boolean function computed at node G in a circuit, and Υ_G is defined inductively as follows. For an input X with label $a \in \{0, 1, x_1, \ldots, x_n\}$, $\Upsilon_X = a$. For a gate G with label ω, if G has m predecessors, say $H_1, \ldots, H_m$, then ω is an operation of m variables and

$$\Upsilon_G = \omega(\Upsilon_{H_1}, \ldots, \Upsilon_{H_m}) \,.$$

Let $F = (f_1, \ldots, f_m)$ be a collection of Boolean functions f_j for $1 \leq j \leq m$. A circuit

is said to *compute* F if the circuit consists of m output gates, say $G_1, \ldots, G_m$, and f_j is the function computed at the output gate G_j, i.e., $\Upsilon_{G_j} = f_j$ for $1 \leq j \leq m$.

The *size* of a circuit is the number of gates in it. The *depth* of a circuit is the length (number of edges) of the longest directed path from an input to an output gate. The *size complexity* of F is the minimum size of circuits computing F. Similarly, the *depth complexity* of F is the minimum depth of circuits computing F.

In this thesis, we consider two types of circuits. First, we consider the circuits over basis $\{\wedge, \vee, \neg\}$, called *Boolean circuits*, where $\wedge$ and $\vee$ are respectively conjunction and disjunction of 2 variables. The $\wedge$ gates and the $\vee$ gates are called *monotone gates*, and the $\neg$ gates are called *negation gates*. We also consider the *threshold circuits*. In a *threshold circuit*, each gate computes a *weighted threshold function* or *negation of a weighted threshold function*. A *weighted threshold function* f is a Boolean function defined as follows: There exist $n+1$ non-negative integers $w_1, \ldots, w_n, t$ such that

$$f(x) = 1 \quad \text{if and only if} \quad w_1 x_1 + \cdots + w_n x_n \geq t\,.$$

A gate computes a weighted threshold function is called a *monotone gate*, and a gate computes negation of a weighted threshold function is called a *negation gate*.

Chapter 3

Negation-limited Boolean circuits

3.1 Negation-limited Boolean circuits

In this chapter, circuits over basis $\{\wedge, \vee, \neg\}$ each of which contains minimum number of negations, the *negation-limited circuits*, are considered. We first show some properties of negation-limited circuits. By using such properties we show some bounds on size and depth of negation-limited circuits.

Markov [11] defined for any collection of Boolean functions F, the *inversion complexity* of F, denoted by $I(F)$, as the *minimum number of negations* contained in circuits computing F.

Theorem 3.1.1 (Markov [11]) *For any collection of Boolean functions F,*

$$I(F) = \lceil \log(d(F) + 1) \rceil .$$

A Boolean circuit contains at most r negations is called an *r-circuit*. Especially, a 0-circuit is commonly called a *monotone circuit*. A $I(f)$-circuit computing F is called a *negation-limited circuit computing F*.

3.1.1 Notations

Let $F = (f_1, \ldots, f_m)$ be an arbitrary collection of Boolean functions. By $C(F)$ (or $C(f_1, \ldots, f_m)$), we denote the *size complexity of F*. By $D(F)$ (or $D(f_1, \ldots, f_m)$), we denote the *depth complexity of F*.

By $C^r(F)$ (or $C^r(f_1, \ldots, f_m)$) we denote the minimum size of r-circuits computing F. Similarly, by $D^r(F)$ (or $D^r(f_1, \ldots, f_m)$) we denote the minimum depth of r-circuits computing F. Note that $C^r(F)$ and $D^r(F)$ are defined only for $r \geq I(F)$. If $r = I(F)$, we call respectively $C^r(F)$ and $D^r(F)$ the *negation-limited size complexity* and the *negation-limited depth complexity* of F.

3.2 Properties of negation-limited circuits

Tanaka and Nishino [18], and Beals, Nishino and Tanaka [4] showed some properties of negation-limited circuits for some class of Boolean functions (symmetric functions and inverters). They showed that if the maximum number of decreases of those functions are power of 2, then the Boolean function computed at each negation gate can be determined. By using such properties, lower bounds of size and depth are shown.

We show that such properties are also valid for negation-limited circuits computing some collections of Boolean functions.

Let $F = (f_1, \ldots, f_m)$ be an arbitrary collection of Boolean functions with $d(F)+1 = 2^r$ for some integer $r \geq 1$, i.e., by Theorem 3.1.1 $r = I(F)$. Let $\alpha = (\alpha^0, \ldots, \alpha^n)$ be a chain such that $|dec(F, \alpha)| = d(F)$. Assume without loss of generality that (by renumbering the variables) $\alpha_i^l = 1$ for $i \leq l$, and $\alpha_i^l = 0$ otherwise, i.e.,

$$\alpha^l = (\overbrace{1, \ldots, 1}^{1^l}, \overbrace{0, \ldots, 0}^{0^{n-l}}) .$$

Let $d_F^\alpha(j)$ be the number of elements in $dec(F, \alpha)$ which is not larger than j, i.e.,

$$d_F^\alpha(j) = |\{\, l \in dec(F, \alpha) \,|\, l \geq j \,\}|$$

for $1 \leq j \leq n$. It is obvious that $d_F^\alpha(j) \leq d_F^\alpha(i)$ if and only if $j \leq i$. Note that the smallest index j such that $d_F^\alpha(j) = l$ for $1 \leq l \leq d(f)$ is the l-th smallest element of $dec(F, \alpha)$.

By $N_1, \ldots, N_r$ we denote the r negation gates in an arbitrary r-circuit such that there is no path from N_i to N_j if $i > j$. By Z_i for $1 \leq i \leq r$ we denote the predecessor of N_i. Then $\Upsilon_{Z_i} = \neg \Upsilon_{N_i}$. Since there is no path from any negation gates to N_1, Z_1 is a monotone

gate and Υ_{Z_1} is computed in a monotone subcircuit. By Theorem 3.1.1, Υ_{Z_1} is monotone since $d(\Upsilon_{Z_1}) = 0$.

Lemma 3.2.1 *$(\Upsilon_{Z_1}(\alpha^i), \ldots, \Upsilon_{Z_r}(\alpha^i))$ is the binary representation of $d_F^\alpha(i)$ for $0 \leq i \leq n$.*

Proof. We first show that $\Upsilon_{Z_1}(\alpha^i)$ is the first bit of binary representation of $d_F^\alpha(i)$, i.e., $\Upsilon_{Z_1}(\alpha^i) = 1$ if and only if $d_F^\alpha(i) \geq (d(F)+1)/2$. Let j be the smallest index such that $\Upsilon_{Z_1}(\alpha^j) = 1$ (i.e., $inc(\Upsilon_{Z_1}, \alpha) = \{\, j \,\}$). Since Υ_{Z_1} is monotone, we have $\Upsilon_{Z_1}(\alpha^i) = 1$ if and only if $i \geq j$. By replacing $x_1, \ldots, x_j$ by 1 and N_1 by 0, we obtain an $(r-1)$-circuit computing a collection of Boolean functions F', where $F'(\alpha^i) = F(\alpha^i)$ if $i \geq j$, and $F'(\alpha^i) = F(\alpha^j)$ otherwise. Thus, $dec(F', \alpha) = \{\, i \in dec(F, \alpha) \mid i > j \,\}$. Similarly, by replacing $x_j, \ldots, x_n$ by 0 and N_1 by 1, we obtain an $(r-1)$-circuit computing a collection of Boolean functions F'', where $F''(\alpha^i) = F(\alpha^i)$ if $i \leq j-1$, and $F''(\alpha^i) = F(\alpha^{j-1})$ otherwise. Thus, $dec(F'', \alpha) = \{\, i \in dec(F, \alpha) \mid i < j \,\}$. Since F' and F'' are computed by $(r-1)$-circuits, by Theorem 3.1.1 we have $d(F'), d(F'') \leq 2^{r-1} - 1 = (d(F)-1)/2$. Also note that $dec(F, \alpha) \subseteq dec(F', \alpha) \cup dec(F'', \alpha) \cup \{\, j \,\}$ and $dec(F', \alpha)$, $dec(F'', \alpha)$ and $\{\, j \,\}$ are pairwise disjoint. It implies that $d(F') = |dec(F', \alpha)| = (d(F)-1)/2$ and $d(F'') = |dec(F'', \alpha)| = (d(F)-1)/2$. Hence, we have $j \in dec(F, \alpha)$, and $d_F^\alpha(j) = |dec(F'', \alpha)| + 1 = (d(F)+1)/2$, i.e., $d_F^\alpha(i) \geq d_F^\alpha(j) = (d(F)+1)/2$ for $i \geq j$. Therefore, $\Upsilon_{Z_1}(\alpha^i)$ is the first bit of binary representation of $d_F^\alpha(i)$.

Then, we prove the lemma by induction on r.

Base: $r = 1$, i.e., $d(F) = 1$. It is clear from the above argument, i.e., $\Upsilon_{Z_1}(\alpha^i)$ is the first bit of binary representation of $d_F^\alpha(i)$.

Induction: Suppose the lemma is satisfied for the case $r-1$. From the above argument, we have $\Upsilon_{Z_1}(\alpha^i)$ is the first bit of binary representation of $d_F^\alpha(i)$. Since $d(F')$ $(= d(F''))$ is equal to $(d(F)-1)/2 = 2^{r-1} - 1$, by induction hypothesis $(\Upsilon_{Z_2}(\alpha^i), \ldots, \Upsilon_{Z_r}(\alpha^i))$ is the binary representation of $d_{F'}^\alpha(i)$ $(d_{F''}^\alpha(i))$ if $i \geq j$ $(i < j)$. Note that $d_F^\alpha(i) = (d(F)+1)/2 + d_{F'}^\alpha(i)$ if $i \geq j$, and $d_F^\alpha(i) = d_{F'}^\alpha(i)$ otherwise. It implies that $(\Upsilon_{Z_2}(\alpha^i), \ldots, \Upsilon_{Z_r}(\alpha^i))$ is the binary representation of $d_F^\alpha(i) - (d(f)+1)/2$ for $i \geq j$, and $d_F^\alpha(i)$ otherwise. ∎

From this lemma, we have for any $1 \leq i < j \leq r$

$$\Big(inc(\Upsilon_{Z_i}, \alpha) \cup dec(\Upsilon_{Z_i}, \alpha) \Big) \subseteq dec(\Upsilon_{Z_j}, \alpha)\,.$$

Since $dec(f, \alpha) \cap inc(f, \alpha) = \emptyset$ for any Boolean function f, for any $1 \leq i < j \leq r$

$$\Big(inc(\Upsilon_{Z_i}, \alpha) \cup dec(\Upsilon_{Z_i}, \alpha) \Big) \cap inc(\Upsilon_{Z_j}, \alpha) = \emptyset\,.$$

Let l_j be the j-th smallest element in $dec(F, \alpha)$ for $1 \leq j \leq d(F)$, and let $k = 2^{r-i}$. Then, for $1 \leq i \leq r$, the satisfying set of Υ_{Z_i} over chain α is

$$S(\Upsilon_{Z_i}, \alpha) = [\, l_k, l_{2k}\,) \cup [\, l_{3k}, l_{4k}\,) \cup \cdots \cup [\, l_{(2^i-1)k}, n+1\,)\,,$$

where $[\, i, j\,)$ denote the set $\{\, i, i+1, \ldots, j-1\,\}$ if $i < j$, and $[\, i, j\,) = \emptyset$ otherwise. The lower bounds on size and depth will be shown based on this lemma.

3.3 Lower bounds on negation-limited circuits

In this section, we show lower bounds on depth and size of negation-limited circuits by using the properties of negation-limited circuits shown in the previous section.

3.3.1 Lower bound on depth

Lemma 3.3.1 *There exists a path from N_i to N_{i+1} for $1 \leq i \leq r-1$.*

Proof. Suppose such a path does not exist. Then, $\Upsilon_{Z_{i+1}}$ is a monotone function of x and $\Upsilon_{N_1}(x), \ldots, \Upsilon_{N_{i-1}}(x)$. Let $k > k'$ be integers such that $d_F^\alpha(k) = 2^{r-i}$ and $d_F^\alpha(k') = 2^{r-i-1}$. From Lemma 3.2.1, we have $\Upsilon_{Z_{i+1}}(\alpha^k) = 0$ and $\Upsilon_{Z_{i+1}}(\alpha^{k'}) = 1$. Note that $\alpha^k \geq \alpha^{k'}$, and $\Upsilon_{N_j}(\alpha^k) = \Upsilon_{N_j}(\alpha^{k'}) = 0$ for $j < i$ (from Lemma 3.2.1). From the monotonicity of $\Upsilon_{Z_{i+1}}$, we have $\Upsilon_{Z_{i+1}}(\alpha^k) \geq \Upsilon_{Z_{i+1}}(\alpha^{k'}) = 1$. Therefore, there exists a path from N_i to N_{i+1}. ∎

Since there is no path from N_i to N_j if $i > j$, any path from N_i to N_{i+1} does not contain any negation gate except N_i and N_{i+1}. Thus, $Z_2, \ldots, Z_r$ are monotone gates.

Lemma 3.3.2 *On any path from N_i to N_{i+1} for $1 \leq i \leq r-1$, there are at least one $\wedge$ gate and at least one $\vee$ gate.*

Proof. From Lemma 3.2.1, there are four different pairs for $(\Upsilon_{Z_i}(\alpha^j), \Upsilon_{Z_{i+1}}(\alpha^j))$ for $0 \leq j \leq n$. Suppose there exists a path from N_i to N_{i+1} consists only of $\wedge$ gate ($\vee$ gate). Then, $\Upsilon_{Z_{i+1}}(\alpha^j) = \Upsilon_{N_i}(\alpha^j) = 0$ if $\Upsilon_{Z_i}(\alpha^j) = 1$. It implies that $(\Upsilon_{Z_i}(\alpha^j), \Upsilon_{Z_{i+1}}(\alpha^j)) \neq (1,1)$ $((\Upsilon_{Z_i}(\alpha^j), \Upsilon_{Z_{i+1}}(\alpha^j)) \neq (0,0))$ for any $1 \leq j \leq n$.

Therefore, any path from N_i to N_{i+1} consists of at least one $\wedge$ gate and at least one $\vee$ gate. ∎

From Lemma 3.3.1 and 3.3.2, a lower bound on depth of r-circuits computing F is obtained.

Theorem 3.3.3 *Let F be an arbitrary collection of Boolean functions with $d(F)+1 = 2^r$. Then,*

$$D^r(F) \geq D^0(\Upsilon_{Z_1}) + 3r - 2\,.$$

Proof. Since Υ_{Z_1} is computed in a monotone subcircuit, there exists a path with length at least $D^0(\Upsilon_{Z_1})$ from some input to Z_1. From Lemma 3.3.1 and 3.3.2, there exists a path with length at least $3r-2$ from N_1 to N_r. Therefore, there exists a path with length at least $D^0(\Upsilon_{Z_1}) + 3r - 2$ in r-circuits computing F. ∎

For Boolean functions, the lower bound on depth can be improved. Let f be a Boolean function with $d(f) + 1 = 2^r$ for some $r \geq 2$. By Z_{r+1} , we denote the output gate of an r-circuit computing f, i.e., $\Upsilon_{Z_{r+1}} = f$. Note that in all r-circuits computing f, there exists a path from N_r to Z_{r+1}.

Lemma 3.3.4 *There exists a path from N_r to Z_{r+1}.*

Since there is no path from N_r to N_i for $i < r$, any path from N_r to the output gate does not contain any negation gate except N_r.

Lemma 3.3.5 *On any path from N_r to Z_{r+1}, there are at least one $\wedge$ gate and at least one $\vee$ gate.*

Proof. By the same argument of Lemma 3.3.2, it is sufficient to show that there are four different pairs for $(\Upsilon_{Z_r}(\alpha^j), f(\alpha^j))$ for $0 \leq j \leq n$. From Lemma 3.2.1, we have $j \in dec(f, \alpha)$ if and only if $j \in dec(\Upsilon_{Z_r}, \alpha) \cup inc(\Upsilon_{Z_r}, \alpha)$ (i.e., $\Upsilon_{Z_r}(\alpha^{j-1}) \neq \Upsilon_{Z_r}(\alpha^j)$). It implies that $(\Upsilon_{Z_r}(\alpha^j), f(\alpha^j)) = (1,0)$ for $j \in inc(\Upsilon_{Z_r}, \alpha)$ and $(\Upsilon_{Z_r}(\alpha^j), f(\alpha^j)) = (0,0)$ for $j \in dec(\Upsilon_{Z_r}, \alpha)$. It also implies that $(\Upsilon_{Z_r}(\alpha^{j-1}), f(\alpha^{j-1})) = (0,1)$ for $j \in inc(\Upsilon_{Z_r}, \alpha)$ and $(\Upsilon_{Z_r}(\alpha^{j-1}), f(\alpha^{j-1})) = (1,1)$ for $j \in dec(\Upsilon_{Z_r}, \alpha)$. Since $r \geq 2$, i.e., $d(f) \geq 3$, we have $inc(\Upsilon_{Z_r}, \alpha) \neq \emptyset$ and $dec(\Upsilon_{Z_r}, \alpha) \neq \emptyset$. ∎

Note that from this lemma the output gate Z_{r+1} is a monotone gate. From Theorem 3.3.3, Lemma 3.3.4 and 3.3.5, we have the following theorem.

Theorem 3.3.6 *Let f be an arbitrary Boolean function with $d(f) + 1 = 2^r$ for $r \geq 2$. Then,*

$$D^r(f) \geq D^0(\Upsilon_{Z_1}) + 3r\,. \qquad \blacksquare$$

3.3.2 Lower bound on size

We denote by $\Delta(G)$ and $\nabla(G)$ respectively the set of all *ancestors* and the set of all *descendants* of a gate G in a circuit. The set $\Delta(G)$ consists only of G and all ancestors of predecessors of G except inputs, and the set $\nabla(G)$ consists only of G and all descendants of successors of G. By $\overline{\nabla(G)}$ we denote the complement of $\nabla(G)$, i.e., $\overline{\nabla(G)}$ consists of all gates which are not in $\nabla(G)$. We show a lower bound on size of r-circuit computing f in the following form.

$$C^r(f) \geq |\overline{\nabla(N_1)}| + |\nabla(N_1)|\,.$$

Since $\overline{\nabla(N_1)}$ does not contain any negation gate, $\Upsilon_{Z_1} \in \overline{\nabla(N_1)}$ is computed by a monotone subcircuit in $\overline{\nabla(N_1)}$. Thus, we have $|\overline{\nabla(N_1)}| \geq C^0(\Upsilon_{Z_1})$. It implies that

$$C^r(f) \geq C^0(\Upsilon_{Z_1}) + |\nabla(N_1)|\,.$$

In the following, we show the lower bound on $|\nabla(N_1)|$.

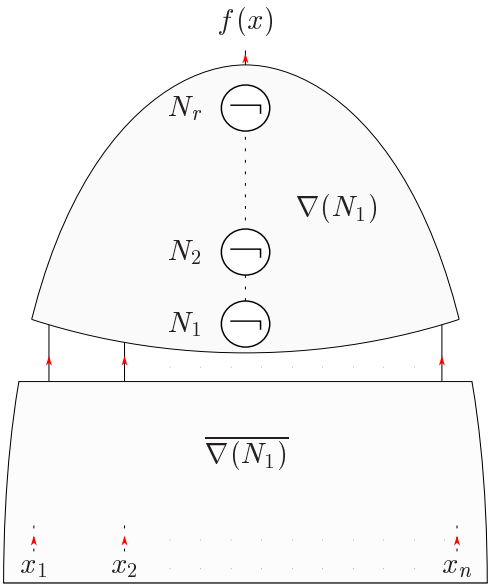

Figure 3.1: Separation of $\overline{\nabla(N_1)}$ and $\nabla(N_1)$ in an r-circuit computing f

Lemma 3.3.7

(i) *If* $G \in \nabla(N_1)$, *then* $\nabla(G) \subseteq \nabla(N_1)$.

(ii) *If* $G \in \nabla(N_1) - \{N_1\}$, *then at least one predecessor of* G *is in* $\nabla(N_1)$.

(iii) $N_i, \ldots, N_r, Z_{i+1}, \ldots, Z_{r+1}$ *are in* $\nabla(N_i)$.

(iv) *If* $G \in \overline{\nabla(N_1)}$, *then* Υ_G *is monotone.*

Proof. (i) and (ii) are obvious. (iii) follows directly from Lemma 3.3.1 and 3.3.4.

(iv) For any gate $G \in \overline{\nabla(N_1)}$, $\Delta(G)$ does no contain any negation gate. Therefore, Υ_G is computed in a monotone subcircuit, i.e., Υ_G is a monotone. ∎

Since the number of negation gates, r, is known, we consider the number of monotone gates in $\nabla(N_1)$. From (ii) of Lemma 3.3.7, we can distinguish the monotone gates in $\nabla(N_1)$ in the following ways. A monotone gate $G \in \nabla(N_1)$ is called an *internal gate* if both predecessors of G are in $\nabla(N_1)$. Otherwise, i.e., exactly one predecessor of G is in $\nabla(N_1)$, G is called a *boundary gate* (G is at the boundary of $\nabla(N_1)$ and $\overline{\nabla(N_1)}$).

Lemma 3.3.8

(i) For any monotone gate G and any $i \in inc(\Upsilon_G, \alpha)$, there exists a predecessor H of G which satisfies $i \in inc(\Upsilon_H, \alpha)$.

(ii) For any gate G which satisfies $G \in \Delta(Z_i)$ and $inc(\Upsilon_G, \alpha) \cap inc(\Upsilon_{Z_i}, \alpha) \neq \emptyset$ for some $2 \leq i \leq r+1$, then G is a monotone gate.

Proof. (i) Let H_1 and H_2 be the predecessors of G. Suppose $i \notin inc(\Upsilon_{H_1}, \alpha) \cup inc(\Upsilon_{H_2}, \alpha)$. It implies that $\Upsilon_{H_1}(\alpha^{i-1}) \geq \Upsilon_{H_1}(\alpha^i)$ and $\Upsilon_{H_2}(\alpha^{i-1}) \geq \Upsilon_{H_2}(\alpha^i)$. Since G is a monotone gate, we have $\Upsilon_G(\alpha^{i-1}) \geq \Upsilon_G(\alpha^i)$. It implies that $i \notin inc(\Upsilon_G, \alpha)$. Therefore, if $i \in inc(\Upsilon_G, \alpha)$, there exists a predecessor H of G which satisfies $i \in inc(\Upsilon_H, \alpha)$.

(ii) Since $G \in \Delta(Z_i)$ and $N_j \notin \nabla(Z_i)$ for $j \geq i$, we have $G \neq N_j$ for $j \geq i$. From Lemma 3.2.1, we have for $1 \leq j < i$,

$$\Big(inc(N_j, \alpha) \cup dec(N_j, \alpha)\Big) \cap inc(\Upsilon_{Z_i}, \alpha) = \emptyset\,.$$

Since $inc(N_j, \alpha) \cup dec(N_j, \alpha) \subseteq dec(f, \alpha) = dec(\Upsilon_{Z_{r+1}}, \alpha)$ for $1 \leq j \leq r$, we have

$$\Big(inc(N_j, \alpha) \cup dec(N_j, \alpha)\Big) \cap inc(\Upsilon_{Z_{r+1}}, \alpha) = \emptyset\,.$$

Then, from the assumption $inc(\Upsilon_G, \alpha) \cap inc(\Upsilon_{Z_i}, \alpha) \neq \emptyset$, we have $inc(\Upsilon_G, \alpha) \neq inc(\Upsilon_{N_j}, \alpha)$ for $j < i$. It implies that $G \neq N_j$ for $j < i$. ■

Then we have the following lemma.

Lemma 3.3.9 *For each $l \in \bigcup_{i=2}^{r+1} inc(\Upsilon_{Z_i}, \alpha)$, there exists a path P which satisfies the following conditions.*

(i) The terminal of P is Z_i for some $2 \leq i \leq r+1$.

(ii) For each gate G on P, G is a monotone gate in $\nabla(N_1)$ and satisfies $l \in inc(\Upsilon_G, \alpha)$.

(iii) The source of P is a boundary gate, where the predecessor G of the source of P which is in $\nabla(N_1)$ satisfies $l \notin inc(\Upsilon_G, \alpha)$.

We call such a path P, an *l-path*, for each $l \in \bigcup_{i=2}^{r+1} inc(\Upsilon_{Z_i}, \alpha)$. Note that for the predecessor G of a boundary gate such that $G \in \overline{\nabla(N_1)}$, Υ_G is monotone, i.e., $|inc(\Upsilon_G, \alpha)| \leq 1$ and $dec(\Upsilon_G, \alpha) = \emptyset$. A boundary gate is called an *l-boundary gate* if whose predecessor G in $\overline{\nabla(N_1)}$ satisfies $inc(\Upsilon_G, \alpha) = \{ l \}$. Then, the source of an l-path is an l-boundary gate. We show that for each $l \in \bigcup_{i=2}^{r+1} inc(\Upsilon_{Z_i}, \alpha)$ there exists an l-boundary gate as the source of l-path. Let

$$M = |inc(f, \alpha) \cup dec(f, \alpha)| .$$

In terms of M, the following lemmas are shown.

Lemma 3.3.10 *There are at least $M - 1$ boundary gates in $\nabla(N_1)$.*

Proof. It is obvious that for any $l \neq l'$, a boundary gate cannot be an l-boundary gate and an l'-boundary gate simultaneously. Hence, it is sufficient to show that there are at least $M - 1$ l-path's with different l.

From Lemma 3.3.9, there exists an l-path for each $l \in \bigcup_{i=2}^{r+1} inc(\Upsilon_{Z_i}, \alpha)$. Since from Lemma 3.2.1, we have

$$dec(f, \alpha) = \bigcup_{i=1}^{r} inc(\Upsilon_{Z_i}, \alpha)$$

and $inc(\Upsilon_{Z_{r+1}}, \alpha) = inc(f, \alpha)$. Hence,

$$dec(f, \alpha) \cup inc(f, \alpha) = \bigcup_{i=1}^{r+1} inc(\Upsilon_{Z_i}, \alpha) ,$$

Again from Lemma 3.2.1 we have $|inc(\Upsilon_{Z_1}, \alpha)| = 1$. Therefore, there are at least

$$\left| \bigcup_{i=2}^{r+1} inc(\Upsilon_{Z_i}, \alpha) \right| = M - 1$$

boundary gates. ∎

For each $l \in \bigcup_{i=2}^{r+1} inc(\Upsilon_{Z_i}, \alpha)$, on l-path, we call the first internal gate from source, G_l, and the predecessor of G_l on l-path, H_l. If l-path does not contain any internal gate, then G_l is undefined and H_l is the terminal of l-path, i.e., $H_l = Z_i$ such that $l \in inc(\Upsilon_{Z_i}, \alpha)$. By $\hat{G}$ we denote the set of all G_l, and by $\hat{H}$ we denote the set of all H_l. Note that $\hat{G} \cap \hat{H} = \emptyset$

since each $H \in \hat{H}$ is a boundary gate. We will show the lower bound of $|\hat{G}|$ as a lower bound of the number of internal gates in $\nabla(N_1)$.

For a boundary gate H, by B_H we denote that path which consists of only boundary gates such that a predecessor of source of B_H is an internal gate, and B_H is terminate at H. Note that such a path B_H is unique, since each boundary gate has exactly one predecessor in $\nabla(N_1)$, we can find the source of B_H by backtracking from H.

For $H \in \hat{H}$, if $H = H_l$, then the source of l-path is on B_H, and we have $l \in inc(\Upsilon_H, \alpha)$. Then we find the number of $l \in \bigcup_{i=2}^{r+1} inc(\Upsilon_{Z_i}, \alpha)$ such that $H = H_l$, i.e., the number of $l \in \bigcup_{i=2}^{r+1} inc(\Upsilon_{Z_i}, \alpha)$ such that source of l-path is on B_H.

Suppose B_H consists of k boundary gates (including H). For $1 \leq i \leq k$ by F_i we denote the predecessor of the i-th gate on B_H which is in $\overline{\nabla(N_1)}$, and by G we denote the predecessor of the source of B_H other than F_1. Then Υ_H can be represented in following form.

$$\Upsilon_H = \Upsilon_{F_k} *_k (\Upsilon_{F_{k-1}} *_{k-1} (\ldots (\Upsilon_{F_1} *_1 \Upsilon_G))),$$

where $*_i \in \{\wedge, \vee\}$ for $1 \leq i \leq k$ is the type of the i-th gate on B_H. Since $F_i \in \overline{\nabla(N_1)}$, i.e., Υ_{F_i} is monotone, we have $S(\Upsilon_{F_i}, \alpha) = [\, l, n+1)$ for some $1 \leq l, n+1$, i.e., $|inc(\Upsilon_{F_i}, \alpha)| = 1$. Then, if F_i is a source of an l-path passing through H, then $l = inc(\Upsilon_H, \alpha) \cap inc(\Upsilon_{F_i}, \alpha)$, and

$$l \notin inc\Big(\Upsilon_{F_{i-1}} *_{i-1} (\Upsilon_{F_{k-1}} *_{k-1} (\ldots (\Upsilon_{F_1} *_1 \Upsilon_G))), \alpha\Big).$$

For arbitrary Boolean functions g_1 and g_2, we denote $S(g_1, \alpha) = S(g_2, \alpha)$ by $g_1 \equiv^\alpha g_2$. Let h_l for $1 \leq l \leq n$ be a Boolean function such that $S(h_l, \alpha) = [\, l, n+1\,)$.

Lemma 3.3.11 *Let g be an arbitrary Boolean function, and let $*_1, \ldots, *_k \in \{\wedge, \vee\}$ and $1 \leq l_1, \ldots, l_k \leq n$. Then,*

$$h_{l_k} *_k (h_{l_{k-1}} *_{k-1} (\ldots (h_{l_1} *_1 g))) \equiv^\alpha h_{l_i} *_i (h_{l_j} *_j g).$$

for some $1 \leq i, j \leq k$.

Proof. Let g' be an arbitrary Boolean function. We show that for $k \geq 3$ one of h_k, h_{k-1}, h_{k-2} can be eliminated without changing the satisfying set.

Case 1. $*_k = *_{k-1}$. If $*_k = *_{k-1} = \wedge$, then $h_{l_k} \wedge (h_{l_{k-1}} \wedge g') \equiv^\alpha h_l \wedge g'$ for $l = \max\{\, l_k, l_{k-1} \,\}$, since

$$S\Big((h_{l_k} \wedge (h_{l_{k-1}} \wedge g')), \alpha\Big) = \Big(S(g', \alpha) - [\, 0, l_{k-1}\,)\Big) - [\, 0, l_k\,) = S(g', \alpha) - [\, 0, l\,)\,.$$

Similarly, if $*_k = *_{k-1} = \vee$, $h_{l_k} \vee (h_{l_{k-1}} \vee g') \equiv^\alpha h_l \vee g'$ for $l = \min\{\, l_k, l_{k-1} \,\}$.

Case 2. $*_k = *_{k-2}$ and $*_k \neq *_{k-1}$. Suppose $*_k = *_{k-2} = \wedge$ and $*_{k-1} = \vee$. Then

$$S\Big((h_{l_k} \wedge (h_{l_{k-1}} \vee (h_{l_{k-2}} \wedge g'))), \alpha\Big) = \Big(\Big(S(g', \alpha) - [\, 0, l_{k-2}\,)\Big) \cup [\, l_{k-1}, n+1\,)\Big) - [\, 0, l_k\,)\,.$$

If $l_k \geq l_{k-2}$, then $h_{l_k} \wedge (h_{l_{k-1}} \vee (h_{l_{k-2}} \wedge g')) \equiv^\alpha h_{l_k} \wedge (h_{l_{k-1}} \vee g')$, since

$$S\Big((h_{l_k} \wedge (h_{l_{k-1}} \vee (h_{l_{k-2}} \wedge g'))), \alpha\Big) = \Big(S(g', \alpha) \cup [\, l_{k-1}, n+1\,)\Big) - [\, 0, l_k\,)\,.$$

If $l_{k-1} \leq l_k$, then $h_{l_k} \wedge (h_{l_{k-1}} \vee g')) \equiv^\alpha h_{l_k}$, since

$$\Big(S(g', \alpha) \cup [\, l_{k-1}, n+1\,)\Big) - [\, 0, l_k\,) = [l_k, n+1) = S(h_{l_k}, \alpha)\,.$$

Thus, we have $h_{l_k} \wedge (h_{l_{k-1}} \vee (h_{l_{k-1}} \wedge g')) \equiv^\alpha h_{l_k} \wedge (h_{l_{k-1}} \vee g')$. If $l_{k-1}, l_{k-2} > l_k$, then $h_{l_k} \wedge (h_{l_{k-1}} \vee (h_{l_{k-2}} \wedge g')) \equiv^\alpha h_{l_{k-1}} \vee (h_{l_{k-2}} \wedge g')$, since

$$S\Big((h_{l_k} \wedge (h_{l_{k-1}} \vee (h_{l_{k-2}} \wedge g'))), \alpha\Big) = \Big(S(g', \alpha) - [\, 0, l_{k-2}\,)\Big) \cup [\, l_{k-1}, n+1\,)\,.$$

Similarly, the case $*_k = *_{k-2} = \vee$ and $*_{k-1} = \wedge$ is also satisfies the lemma.

Case 3. $*_k \neq *_{k-1}$ and $*_{k-1} = *_{k-2}$. By the same argument in *Case 1*, for $*_{k-1} = *_{k-2} = *$ $h_{l_k} *_k (h_{l_{k-1}} * (h_{l_{k-2}} * g')) \equiv^\alpha h_{l_k} *_k (h_l * g')$ where $l = \max\{\, l_{k-1}, l_{k-2}\,\}$ if $* = \wedge$, otherwise $l = \min\{\, l_{k-1}, l_{k-2}\,\}$. ∎

Lemma 3.3.11 implies that at least $|inc(\Upsilon_H, \alpha)| - 2$ increases of Υ_H is also increases of Υ_G. Thus, there are at most 2 source of some l-path are on B_H, i.e., the number of $l \bigcup_{i=2}^{r+1} inc(\Upsilon_{Z_i}, \alpha)$ such that $H_l = H$ is at most 2. It implies that

$$|\hat{H}| \geq (M-1)/2\,.$$

It also implies that the number of $l \in \bigcup_{i=2}^{r+1} inc(\Upsilon_{Z_i}, \alpha)$ such that l-path consists of some internal gate is at least $M - 2r - 1$. Then we show the lower bound of $|\hat{G}|$.

Lemma 3.3.12 *There are at least* $(M-2r-1)/3$ *internal gates in* $\nabla(N_1)$.

Proof. It is sufficient to show that for each $G \in \hat{G}$ the number of $l \in \bigcup_{i=2}^{r+1} inc(\Upsilon_{Z_i}, \alpha)$ such that $G_l = G$ is at most 3.

Suppose $G = G_{l_i}$ for $i = 1, 2, 3, 4$ and $l_i \in \bigcup_{i=2}^{r+1} inc(\Upsilon_{Z_i}, \alpha)$. Let H and H' be the predecessor of G. Then, $H, H' \in \hat{H}$ and for $i \in \{1, 2, 3, 4\}$ $H_{l_i} = H$ or $H_{l_i} = H'$. Assume without loss of generality that $H = H_{l_1} = H_{l_2}$ and $H' = H_{l_3} = H_{l_4}$, and $l_1 < l_2$ and $l_3 < l_4$ Then note that from Lemma 3.3.11, the satisfying set of Υ_H must be as follows. For some Boolean function h,

$$S(\Upsilon_H, \alpha) = (S(h, \alpha) \cup [\, l_2, n+1\,)) - [\, 0, l_1\,)\,.$$

Similarly, for some Boolean function h',

$$S(\Upsilon_{H'}, \alpha) = (S(h', \alpha) \cup [\, l_4, n+1\,)) - [\, 0, l_3\,)\,.$$

If G is an $\wedge$ gate, then

$$\begin{aligned} S(\Upsilon_G, \alpha) &= \Big((S(h, \alpha) \cup [\, l_2, n+1\,)) - [\, 0, l_1\,)\Big) \cap \Big((S(h', \alpha) \cup [\, l_4, n+1\,)) - [\, 0, l_3\,)\Big) \\ &= \Big(S(h, \alpha) \cup [\, l_2, n+1\,)\Big) \cap \Big(S(h', \alpha) \cup [\, l_4, n+1\,)\Big) - [\, 0, l\,)\,, \end{aligned}$$

where $l = \max\{\, l_1, l_3\,\}$. It implies that $\min\{\, l_1, l_3\,\} \notin inc(\Upsilon_G, \alpha)$. Therefore, the number of $l \in \bigcup_{i=2}^{r+1} inc(\Upsilon_{Z_i}, \alpha)$ such that $G_l = G$ is at most 3. Hence,

$$|\hat{G}| \geq (M-2r-1)/3\,.$$

■

Note that all gates on a l-path are monotone gates. Thus, from Lemma 3.3.10 and Lemma 3.3.12, a lower bound of $|\nabla(N_1)|$ is obtained.

$$|\nabla(N_1)| \geq (1+1/3)(M-1) + r/3\,. \tag{3.1}$$

Theorem 3.3.13 *Let* f *be an arbitrary Boolean function with* $d(f)+1 = 2^r$ *for* $r \geq 2$. *Then,*

$$C^r(f) \geq C^0(\Upsilon_{Z_1}) + (1+1/3)(M-1) + r/3\,. \qquad ■$$

Since $|inc(f,\alpha)| \geq |dec(f,\alpha)| - 1$, we have $M \geq 2d(f) - 1 = 2^{r+1} - 2$. Thus,

$$C^r(f) \geq C^0(\Upsilon_{Z_1}) + (1 + 1/3)(2^{r+1} - 3) + r/3\,.$$

3.4 Negation-limited circuits for symmetric functions

In this section, we consider the complexity of negation limited circuits computing symmetric functions. The complexity of negation-limited circuits computing symmetric functions has been investigated by Tanaka and Nishino [19] (also see [17]).

A Boolean function f is called *symmetric* if $f(x)$ depends only on $\|x\|$. That is, the satisfying sets $S(f,\alpha)$ over all chains α are the same. Let

$$S(f,\alpha) = [l_1, l_2) \cup [l_3, l_4) \cup \cdots \cup [l_{2k-1}, l_{2k})\,.$$

where $0 \leq l_1 < l_2 < \cdots < l_{2k} \leq n+1$. Then, $dec(f,\alpha) = \{\, l_{2i} \mid 1 \leq i \leq k \,\}$ (i.e., $d(f) = k$) if $l_{2k} < n+1$, and $dec(f,\alpha) = \{\, l_{2i} \mid 1 \leq i \leq k-1 \,\}$ (i.e., $d(f) = k-1$) otherwise.

Here, we define some symmetric functions. The j-th threshold function, denoted by T_j^n, is a symmetric function defined as follows.

$$T_j^n(x) = 1 \quad \text{iff} \quad \|x\| \geq j\,.$$

That is, $S(T_j^n,\alpha) = [\,j, n+1\,)$ (i.e., $dec(T_j^n,\alpha) = \emptyset$) for $1 \leq j \leq n$. Thus, we have $I(T_j^n) = 0$ for $1 \leq j \leq n$.

The parity function, denoted by $PARITY^n$, is defined as follows.

$$PARITY^n(x) = \|x\| \bmod 2\,.$$

For even n, $S(PARITY^n,\alpha) = [\,1,2\,) \cup [\,3,4\,) \cup \cdots \cup [\,n-1, n\,)$, otherwise $S(PARITY^n,\alpha) = [\,1,2\,) \cup [\,3,4\,) \cup \cdots \cup [\,n, n+1\,)$. That is, $dec(PARITY^n,\alpha) = \{\, 2j \mid j = 1, 2, \ldots, \lfloor n/2 \rfloor \,\}$. Thus, we have $I(PARITY^n) = \lceil \log(n+1) \rceil - 1$.

For any symmetric function f, the value of $f(x)$ can be represented by threshold functions as follows:

$$f(x) = (T_{l_1}^n(x) + \cdots + T_{l_{2k}}^n(x)) \bmod 2\,. \tag{3.2}$$

That is, $T^n_{l_1}(x) + \cdots + T^n_{l_{2k}}(x)$ is odd if and only if $l_{2j-1} \leq \|x\| < l_{2j}$ for some $1 \leq j \leq k$. Since $T^n_{l_{n+1}} = 0$, any symmetric function f can be represented as mod2 of a sum of at most $2d(f) + 1$ threshold functions.

3.4.1 Upper bounds on size and depth

Theorem 3.4.1 *For an arbitrary symmetric function f with $I(f) = r$,*

(i) $C^r(f) \leq C^0(T^n_{l_1}, \ldots, T^n_{l_{2k}}) + 2^{r+2} - r - 4$,

(ii) $D^r(f) \leq D^0(T^n_{l_1}, \ldots, T^n_{l_{2k}}) + 3r$.

Proof. An r-circuit computing f can be constructed as follows. From (3.2), f can be represented as mod2 of a sum of at most $2d(f) + 1$ threshold functions.

$$f(x) = (T^n_{l_1}(x) + \cdots + T^n_{l_{2d(f)+1}}(x)) \bmod 2\,,$$

where $0 \leq l_1 < \ldots < l_{2d(f)+1} \leq n + 1$. Let us define the functions $f^n_{i,j}$ for $0 \leq i \leq r$ and $1 \leq j < 2^{i+1}$,

$$f^n_{i,j}(x) = 1 \quad \text{if and only if} \quad (T^n_{l_1}(x) + \cdots + T^n_{l_{2d(f)+1}}(x)) \bmod 2^{i+1} \geq j\,.$$

Note that $f^n_{r,j} = T^n_{l_j}$ for $1 \leq j \leq 2d(f) + 1$, and $f^n_{r,j} = 0$ for $2d(f) + 1 < j < 2^{r+1}$. Furthermore, $f^n_{0,1} = f$.

The $f^n_{r,j}$ for all $1 \leq j < 2^{r+1}$ can be computed by a monotone circuit computing a collection of threshold functions $(T^n_{l_1}, \ldots, T^n_{l_{2d(f)+1}})$. We start from $i = r$, given the $f^n_{i,j}$ for all $1 \leq j < 2^{i+1}$, the $f^n_{i-1,j}$ for all $1 \leq j < 2^i$ are computed in depth 3 as follows.

(i,1) Compute $g^n_i = \neg f^n_{i,2^i}$.

(i,2) Compute $h^n_{i,j} = f^n_{i,j} \wedge g^n_i$ for $1 \leq j < 2^i$ in parallel.

(i,3) Compute $f^n_{i-1,j} = h^n_{i,j} \vee f^n_{i,j+2^{i-1}}$ for $1 \leq j < 2^i$ in parallel.

The correctness of above computation can be shown as follows.

1. $g^n_i(x) = 1$ if and only if $(T^n_{l_1}(x) + \cdots + T^n_{l_m}(x)) \bmod 2^{i+1} < 2^i$.

2. $h^n_{i,j}(x) = 1$ if and only if $j \leq (T^n_{l_1}(x) + \cdots + T^n_{l_m}(x)) \bmod 2^{i+1} < 2^i$

3. $f^n_{i-1,j}(x) = 1$ if and only if $j + k2^i \leq (T^n_{l_1}(x) + \cdots + T^n_{l_m}(x)) \bmod 2^{i+1} < (k+1)2^i$ for $k \in \{0, 1\}$.

The step $(i,1)$ is computed by one negation gate. The steps $(i,2)$ and $(i,3)$ are respectively computed by $2^i - 1$ gates of type $\wedge$ and $2^i - 1$ gates of type $\vee$. Therefore, given $T^n_{l_1}, \ldots, T^n_{l_m}$,

$$(2^{r+1} - 2) + (2^r - 2) + \cdots + (2^2 - 2) = 2^{r+2} - 2r - 4$$

monotone gates and r negation gates are used to compute f. ∎

Note that in the circuit constructed above, negation gate N_j for each $1 \leq j \leq r$ is in depth $D^0(T^n_{l_1}, \ldots, T^n_{l_{2d(f)+1}}) + 3j - 2$.

Our upper bound of depth $D^r(f)$ shown in Theorem 3.4.1 matches the lower bound for some symmetric function f such that for l be the 2^{r-1} smallest decrease of f,

$$D^0(T^n_l) = \max\{D^0(T^n_{l_1}), \ldots, D^0(T^n_{l_{2k}})\} = D^0(T^n_{l_1}, \ldots, T^n_{l_{2k}})\,.$$

It is obvious that such symmetric functions exist.

Since from [1] we have

$$C^0(T^n_1, \ldots, T^n_n) = O(n \log n)$$

We have the following corollary.

Corollary 3.4.2 *For any symmetric function f with $I(f) = r$,*

$$C^r(f) = O(n \log n)\,.$$

3.4.2 Lower Bounds on size and depth

Let f be an arbitrary symmetric function with $d(f) + 1 = 2^r$ for some $r \geq 2$. From Lemma 3.2.1, in an arbitrary r-circuit computing f, the Z_1 (the predecessor of N_1) computes T^n_l, where l is the 2^{r-1}-th smallest decrease of f. From Theorem 3.3.6 and 3.3.13, the lower bounds are obtained.

Corollary 3.4.3 *Let f be an arbitrary symmetric function with $d(f)+1=2^r$ for some $r \geq 2$, and let l be the 2^{r-1}-th smallest decrease of f. Then,*

(i) $C^r(f) \geq C^0(T_l^n) + (1+1/3)(2^{r+1}-3) + r/3$,

(ii) $D^r(f) \geq D^0(T_l^n) + 3r$.

We can obtain a $(5+1/3)n$ lower bound on size for $PARITY^n$. For $n+1=2^{r+1}$, we have $I(PARITY^n)=2^r$ and the 2^{r-1}-th smallest decrease of $PARITY^n$ is $\lceil n/2 \rceil$. From Long's result [10],

$$C^0(T^n_{\lceil n/2 \rceil}) \geq 4n\,,$$

we obtain a lower bound on size for $PARITY^n$.

Corollary 3.4.4 *Let $n+1=2^{r+1}$ and $r \geq 2$. Then,*

$$C^r(PARITY^n) \geq (5+1/3)(n-2) + r/3\,.$$

3.4.3 A superlinear lower bound on size

Beals, Nishino and Tanaka [4] showed a superlinear lower bound on size under an assumption.

Proposition 3.4.5 (Beals, Nishino and Tanaka [4]) *Let f be a symmetric function f with $d(f)+1=2^r$ for $r \geq 1$, and $inc(f,\alpha) \cup dec(f,\alpha) = \{l_1, \ldots, l_M\}$ for some chain α. In an arbitrary r-circuit C computing f if each gate in $\nabla(N_1)$ computes a symmetric function, then $\overline{\nabla(N_1)}$ contains a a (monotone) subcircuit computing $(T^n_{l_1}, \ldots, T^n_{l_M})$, i.e.,*

$$|\overline{\nabla(N_1)}|| \geq C^0(T^n_{l_1}, \ldots, T^n_{l_M})\,.$$

Then, from this proposition and (3.1), the following corollary can be obtained.

Corollary 3.4.6 *In an arbitrary r-circuit computing a symmetric function f with $d(f)+1=2^r$, if each gate in $\nabla(N_1)$ computes a symmetric function, then*

$$C^r(f) \geq C^0(T^n_{l_1}, \ldots, T^n_{l_M}) + (1+1/3)(2^{r+1}-3) + r/3\,.$$

Under such an assumption, our upper bound on size (Theorem 3.4.1) is almost optimal for some symmetric functions f such that $d(f)+1 = 2^r$ for $r \geq 2$. That is, the gap between upper bound and lower bound is less than $2M/3$.

3.5 Conclusion

By showing some properties of negation gates, we have obtained a lower bound on the depth and the size of negation-limited circuits. Our lower bound on the depth of negation-limited circuits is tight, since there exists a symmetric function whose upper bound on depth matches the lower bound. From the upper bound on the size of negation-limited circuits computing symmetric function, the number of boundary gates matches the lower bound, and the difference between the upper bound and the lower bound of descendants of the first negation gate N_1 is at most $2n/3$.

From the boundary gate, we have obtained some connection between $\overline{\nabla(N_1)}$ and $\nabla(N_1)$. It seems to be possible to find some other properties of a negation-limited circuit from the boundary of $\overline{\nabla(N_1)}$ and $\nabla(N_1)$. Since from the negation-limited circuits computing $PARITY^n$, most of the gates are in $\overline{\nabla(N_1)}$. Thus, it is important to find some properties of $\overline{\nabla(N_1)}$.

Chapter 4

Negation-limited Inverters

4.1 Inverters

Let $n+1 = 2^r$ for some $r \geq 1$. The *inverter* of n variables

$$NEG^n = (NEG^n_1, \ldots, NEG^n_n)$$

is a collection of n boolean functions, where

$$NEG^n_i(x) = \neg x_i$$

for all $1 \leq i \leq n$. Theorem 3.1.1 implies that r negation gates are necessary and sufficient to compute NEG^n, i.e., $d(NEG^n) = n$ and $I(NEG^n) = \lceil \log(d(NEG^n)+1) \rceil = r$. An r-circuit computing NEG^n is called a *negation-limited inverter*.

Tanaka and Nishino [18] showed the following properties of negation gates in any negation-limited inverter. In an arbitrary negation-limited inverter, we can label the r negation gates as $N_1, \ldots, N_r$ such that there is no path from N_i to N_j if $i > j$. Let Z_i for $1 \leq i \leq r$ be the predecessor of N_i. Then, we have $\Upsilon_{Z_i} = \neg \Upsilon_{N_i}$. We denote by Y_i the i-th output gate for $1 \leq i \leq n$, i.e., $\Upsilon_{Y_i} = NEG^n_i$.

Proposition 4.1.1 (Tanaka and Nishino [18]) *In an arbitrary negation-limited inverter, the following statements hold.*

(i) $(\Upsilon_{Z_1}(x), \Upsilon_{Z_2}(x), \ldots, \Upsilon_{Z_r}(x))$ *is the binary representation of* $\|x\|$, *i.e.,*

$$\sum_{j=1}^{r} \Upsilon_{Z_j}(x) 2^{r-j} = \|x\| .$$

(ii) *There exists a path from* N_j *to* N_{j+1} *for each* $1 \leq j < r$.

(iii) *There exists a path from* N_r *to* Y_i *for each* $1 \leq i \leq n$.

(iv) *On any path of* (ii) *and* (iii)*, there exist at least one* $\wedge$ *gate and at least one* $\vee$ *gate.*

Observe that, from (i) of Proposition 4.1.1,

$$\begin{aligned} \|x\| &= \sum_{j=1}^{r} \Upsilon_{Z_j}(x) 2^{r-j} = \sum_{j=1}^{r} (1 - \Upsilon_{N_j}(x)) 2^{r-j} \\ &\Rightarrow \qquad \|x\| + \sum_{j=1}^{r} \Upsilon_{N_j}(x) 2^{r-j} = 2^r - 1 = n \,. \end{aligned} \tag{4.1}$$

For any $a, a' \in \{0,1\}^n$ such that $\|a\| \leq n - 2^{r-j}$ and $\|a'\| = \|a\| + 2^{r-j}$, we have $\Upsilon_{Z_j}(a) = 0$ if and only if $\Upsilon_{Z_j}(a') = 1$, i.e.,

$$\Upsilon_{N_j}(a) = 1 \quad \text{if and only if} \quad \Upsilon_{N_j}(a') = 0 \,. \tag{4.2}$$

Furthermore, $\Upsilon_{Z_j}(a) = 0$ if and only if $\Upsilon_{Z_{j'}}(a) = \Upsilon_{Z_{j'}}(a')$ for all $j' \neq j$, i.e.,

$$\Upsilon_{N_j}(a) = 1 \quad \text{if and only if} \quad \Upsilon_{N_{j'}}(a) = \Upsilon_{N_{j'}}(a') \quad \text{for all } j' \neq j \,. \tag{4.3}$$

Also note that on any path of (ii) there is no negation gate except N_j and N_{j+1}, and on any path of (iii) there is no negation gate except N_r.

A lower bound on depth of negation-limited inverter is implied from Proposition 4.1.1.

Corollary 4.1.2 (Tanaka and Nishino [18]) *Let* $n + 1 = 2^r$ *for* $r \geq 2$. *Then,*

$$D^r(NEG^n) \geq D^0(T^n_{\lceil n/2 \rceil}) + 3r \,.$$

4.2 Upper bound on depth

In this section, we show an upper bound on depth of negation-limited inverter. From (4.1), NEG^n_i for $1 \leq i \leq n$ can be represented as follows:

$$NEG^n_i(x) = 1 \quad \text{if and only if} \quad \|x\| - x_i + \sum_{j=1}^{r} \Upsilon_{N_j}(x) 2^{r-j} = n \,.$$

From this observation, we obtain the following theorem.

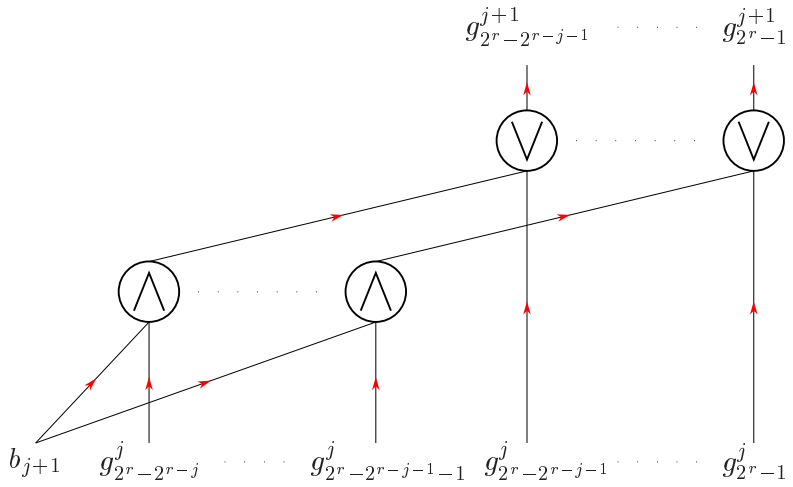

Figure 4.1: Computation of g_k^{j+1} for $0 \leq j < r$ and $2^r - 2^{r-j-1} \leq k < 2^r$.

Theorem 4.2.1 *Let $n+1 = 2^r$ for $r \geq 2$. Then*

$$D^r(NEG^n) \leq D^0(T_1^n, \ldots, T_n^n) + 3r\,.$$

Proof. Let g_k^j be a Boolean function of $n+r$ variables for $0 \leq j \leq r$ and $2^r - 2^{r-j} \leq k < 2^r$ which defined as follows: for $a \in \{0,1\}^n$ and $b \in \{0,1\}^r$,

$$g_k^j(a,b) = 1 \quad \text{if and only if} \quad \|a\| + b_1 2^{r-1} + \cdots + b_j 2^{r-j} \geq k\,.$$

Note that $g_k^0(a,b) = T_k^n(a)$ for $0 \leq k < 2^r$. Therefore, g_k^0 for $0 \leq k < 2^r$ can be computed by depth $D^0(T_1^n, \ldots, T_{2^r-1}^n)$. Also note that we have for $0 \leq j < r$ and $2^r - 2^{r-j-1} \leq k < 2^r$

$$g_k^{j+1} = g_k^j \vee (b_{j+1} \wedge g_{k-2^{r-j-1}}^j)\,,$$

and therefore g_k^{j+1} for $2^r - 2^{r-j-1} \leq k < 2^r$ can be computed by depth 2 if g_k^j for $2^r - 2^{r-j} \leq k < 2^r$ and b_{j+1} are given.

Observe that for each $1 \leq i \leq n$, we have $g_{r,2^r-1}(a,b) = NEG_i^n(x)$, if

$$a = (x_1, \ldots, x_{i-1}, 0, x_{i+1}, \ldots, x_n) \quad \text{and} \quad b = (\Upsilon_{N_1}(x), \ldots, \Upsilon_{N_r}(x))\,.$$

From Theorem 3.4.1, $\Upsilon_{N_j}(x)$ can be computed by depth $D^0(T_1^n, \ldots, T_{2^r-1}^n) + 3j - 2$ for each $1 \leq j \leq r$. Thus, $g_{j,k}$ for $0 \leq j \leq r$ and $2^r - 2^{r-j} \leq k < 2^r$ can be computed by

depth $D^0(T_1^n, \ldots, T_{2^r-1}^n) + 3j$, i.e., $D^r(NEG_i^n) \leq D^0(T_1^n, \ldots, T_{2^r-1}^n) + 3r$ for $1 \leq i \leq n$, and the theorem is proved. ∎

Thus, we have the following corollary from Corollary 4.1.2 and Theorem 4.2.1.

Corollary 4.2.2 *Let $n+1 = 2^r$ for $r \geq 2$. Then*

$$D^r(NEG^n) = D^0(T_{\lceil n/2 \rceil}^n) + 3r$$

if $D^0(T_{\lceil n/2 \rceil}^n) = D^0(T_1^n, \ldots, T_n^n)$.

However, we do not know whether our upper bound on depth matches the lower bound or not, while it is likely to follow that

$$D^0(T_{\lceil n/2 \rceil}^n) = D^0(T_1^n, \ldots, T_n^n)\,.$$

In Section 4.4, we will consider lower bound on size of negation-limited inverter with minimum depth (i.e., $D^r(NEG^n)$) under an assumption $D^0(T_{\lceil n/2 \rceil}^n) = D^0(T_1^n, \ldots, T_n^n)$.

4.3 Lower bound on size

We improve the lower bound on size of negation-limited inverter which shown in [18] by more than $2n$. In [18], a lower bound on size, $5n + 3\log(n+1) - 6$, is shown. That is, $4(n-1)$ gates for $T_{\lceil n/2 \rceil}^n$, $3\log(n+1) - 2$ gates on the path from N_1 to N_r (ii), and the n output gates, Y_i for $1 \leq i \leq n$.

Theorem 4.3.1 *Let $n+1 = 2^r$ for $r \geq 2$. Then,*

$$C^r(NEG^n) \geq (7 + 1/3)n + r/3 - O(1)\,.$$

This theorem is obtained from Corollary 3.4.4, i.e.,

$$C^{r-1}(PARITY^n) \geq (5 + 1/3)n + r/3 - O(1)\,.$$

and the following lemma.

Lemma 4.3.2 *Let $n+1 = 2^r$ for $r \geq 2$. Then,*

$$C^r(NEG^n) \geq C^{r-1}(PARITY^n) + 2n + 1\,.$$

Proof. From (i) of Proposition 4.1.1, we have $\Upsilon_{Z_r} = PARITY^n$. That is, in an arbitrary negation-limited inverter, there exists an $(r-1)$-circuit computing $PARITY^n$ whose output gate is Z_r, the predecessor of N_r. Therefore, it is sufficient to show that there are at least $2n$ gates each of which is on some path from N_r.

Let $a, a' \in \{0,1\}^n$ such that $\|a\| = n$ and $\|a'\| = n-1$ with $a'_i = 0$. Note that Υ_{Y_i} $(= NEG^n_i)$ is a monotone function of x and all Υ_{N_j} for $1 \leq j \leq r$. Also note that $\Upsilon_{Y_i}(a) = 0$ and $\Upsilon_{Y_i}(a') = 1$. From (i) of Proposition 4.1.1, we have $\Upsilon_{N_j}(a) = \Upsilon_{N_j}(a') = 0$ for $1 \leq j < r$, and $0 = \Upsilon_{N_r}(a) \neq \Upsilon_{N_r}(a') = 1$. Since $a > a'$ and $\Upsilon_{Y_i}(a) = 0$, if we fix Υ_{N_r} to 0, from the monotonicity of Υ_{Y_i} we have $\Upsilon_{Y_i}(a') \leq \Upsilon_{Y_i}(a) = 0$. It implies that there exists a path P from N_r to Y_i such that $\Upsilon_G(a') = 1$ for each gate G on P.

Let G be the last $\wedge$ gate on P from N_r to Y_i, i.e., G outputs 1 implies that Y_i outputs 1. We can always find such a gate G from (iv) of Proposition 4.1.1. Note that G is not the last $\wedge$ gate on any path to Y_j for $j \neq i$, since $\Upsilon_G(a') = 1$ and $\Upsilon_{Y_j}(a') = 0$ for $j \neq i$. So, we can find such an $\wedge$ gate G for each $1 \leq i \leq n$, thus, there are at least n $\wedge$ gates each of which is on some paths from N_r.

Similarly, by a dual argument, we can find at least n $\vee$ gates each of which is on some paths from N_r. Therefore, we obtain the lower bound as the lemma stated. ∎

4.4 Size of minimum depth negation-limited inverters

Lower bound on size under an assumption

In this section we will consider the lower bound on size of negation-limited inverters whose depth are minimum (i.e., $D^r(NEG^n)$) under the following natural assumption:

$$D^0(T^n_{\lceil n/2 \rceil}) = D^0(T^n_1, \ldots, T^n_n)\,.$$

In this section, we ignore size and depth of the negation gates. This is a natural formulation, since it can be considered as circuits over basis $\{\wedge, \vee, \overline{\wedge}, \overline{\vee}\}$, where we limit the number of $\overline{\wedge}$ (NAND) and $\overline{\vee}$ (NOR) gates.

Over basis $\{\wedge, \vee, \overline{\wedge}, \overline{\vee}\}$, the minimum depth of negation-limited inverters is

$$D^r(NEG^n) = D^0(T^n_{\lceil n/2 \rceil}) + 2r\,.$$

In any minimum depth negation-limited inverter over basis $\{\wedge, \vee, \overline{\wedge}, \overline{\vee}\}$, N_j is in depth $D^0(T^n_{\lceil n/2 \rceil}) + 2j - 2$ for all $1 \leq j \leq r$. We show that any minimum depth negation-limited inverter over basis $\{\wedge, \vee, \overline{\wedge}, \overline{\vee}\}$ has superlinear size.

Theorem 4.4.1 *If $D^0(T^n_{\lceil n/2 \rceil}) = D^0(T^n_1, \ldots, T^n_n)$, any minimum depth negation-limited inverter over basis $\{\wedge, \vee, \overline{\wedge}, \overline{\vee}\}$ has size at least*

$$2n \log(n+1) + 3n - O(1)\,.$$

In order to show this theorem, we find n disjoint paths in minimum depth negation-limited inverters, and each of these paths consists of $2r - 1$ gates.

For any functions g and g' and a set of assignments $A \subseteq \{0,1\}^n$, we say that $g = g'$ *over* A if and only if $g(a) = g'(a)$ for all $a \in A$. Let $A^j_k \subseteq \{0,1\}^n$ be a set of assignments such that for each $1 \leq j \leq r$ and $0 \leq k < 2^{r-j}$

$$A^j_k = \left\{ a \in \{0,1\}^n \,\middle|\, \|a\| \bmod 2^{r-j} = k \right\}\,.$$

Lemma 4.4.2 *For each $1 \leq i \leq n$, $2 \leq j \leq r$ and $0 \leq k < 2^{r-j}$, any gate G such that $\Upsilon_G = NEG^n_i$ over A^j_k satisfies the following statements.*

(i) *There exists a path from N_j to G which contains no negation gate except N_j.*

(ii) *The path of (i) contains at least one $\wedge$ gate and at least one $\vee$ gate.*

(iii) *There exists exactly one path from N_j to G if G is in depth $D^0(T^n_{\lceil n/2 \rceil}) + 2j$.*

Proof.

(i) Suppose all paths from N_j to G contain of some negation gate others than N_j. Then, Υ_G is a monotone function of x and all N'_j for $j' \neq j$. Let $a, a' \in A^j_k$ such that $a \leq a'$, $\|a\| = k$ with $a_i = 0$, and $\|a'\| = k + 2^{r-j}$ with $a_i = 1$. We show that $\Upsilon_G(a') \neq NEG^n_i(a')$ by the monotonicity of Υ_G, i.e., $a' \geq a$ and $\Upsilon_{N_{j'}}(a') \geq \Upsilon_{N_{j'}}(a)$ for all $j' \neq j$ imply that $\Upsilon_G(a') \geq \Upsilon_G(a)$.

First, we have $a' \geq a$ and $\Upsilon_G(a) = NEG^n_i(a) = 1$. From (i) of Proposition 4.1.1, we have $\Upsilon_{N_j}(a) = 1$ (since $\|a\| = k < 2^{r-j}$). Thus, from (4.3) we have $\Upsilon_{N_{j'}}(a) = \Upsilon_{N_{j'}}(a')$ for all $j' \neq j$. By the monotonicity of Υ_G, we have $\Upsilon_G(a') \geq \Upsilon_G(a) = 1$, while $NEG^n_i(a') = \neg a'_i = 0$.

(ii) Suppose there exists a path from N_j to G where all gates, including G and excluding N_j, are $\wedge$ gates. It implies that $\Upsilon_G(a) = 0$ if $\Upsilon_{N_j}(a) = 0$. It is sufficient to show that there exists an assignment $a \in A^j_k$ such that $\Upsilon_{N_j}(a) = 0$ and $a_i = 0$ (i.e., $\Upsilon_G(a) \neq NEG^n_i(a)$).

From (i) of Proposition 4.1.1, we have $\Upsilon_{N_j}(a) = 0$ for all $a \in \{0,1\}^n$ with $\|a\| = k + 2^{r-j}$. Since all $a \in \{0,1\}^n$ with $\|a\| = k + 2^{r-j}$ are in A^j_k and $k + 2^{r-j} \leq 2^{r-j+1} - 1 < n$ for $j \geq 2$, there exists an assignment $a \in A^j_k$ such that $\|a\| = k + 2^{r-j}$ and $a_i = 0$. For the case that there exists a path from N_j to G where all gates, including G and excluding N_j, are $\wedge$ gates can be proved similarly.

(iii) Since N_j is in depth $D^0(T^n_{\lceil n/2 \rceil}) + 2j - 2$ and G is in depth $D^0(T^n_{\lceil n/2 \rceil}) + 2j$, all paths from N_j to G contain no negation gate except N_j. From (ii), any path from N_j to G contain three gates such that one negation gate N_j, (including G) one $\wedge$ gate and one $\vee$ gate. Thus, there are at most 2 such paths from N_j to G.

Suppose there are 2 paths from N_j to G, i.e., both predecessors of G are successors of N_j. If G is an $\wedge$ gate ($\vee$ gate), then both predecessors of G are $\vee$ gates ($\wedge$ gates). It implies that if $\Upsilon_{N_j}(a) = 1$ $(= 0)$ both predecessors of G output 1 (output 0) and $\Upsilon_G(a) = 1$ $(= 0)$. By the same argument of (ii), it contradicts the assumption of the lemma. ∎

Let G be a gate in depth $D^0(T^n_{\lceil n/2 \rceil}) + 2j$ such that $\Upsilon_G = NEG^n_i$ over A^j_k for some fixed $2 \leq j \leq r$ and $0 \leq k < 2^{r-j}$. From Lemma 4.4.2, there exists exactly one path from N_j to G which contains N_j, and (including G) exactly one $\wedge$ gate and one $\vee$ gate. Let G' be the gate between N_j and G. Thus, G' is in depth $D^0(T^n_{\lceil n/2 \rceil}) + 2j - 1$. Let H be the predecessor of G other than G', and H' be the predecessor of G' other than N_j. Note that Υ_H and $\Upsilon_{H'}$ are monotone functions of x and all $\Upsilon_{N_{j'}}$ for $1 \leq j' < j$, since there is no path from $N_{j''}$ to H or H' for all $j \leq j'' \leq r$.

Lemma 4.4.3 *$\Upsilon_H \wedge \Upsilon_{N_j} = 0$ over A^j_k if G is an $\vee$ gate.*

Proof. Since G is an $\vee$ gate, G' is an $\wedge$ gate, and we have $\Upsilon_G = \Upsilon_H \vee (\Upsilon_{H'} \wedge \Upsilon_{N_j})$. Suppose there exists an assignment $a \in A^j_k$ such that $\Upsilon_H(a) = \Upsilon_{N_j}(a) = 1$. It implies that $\Upsilon_G(a) = NEG^n_i(a) = 1$, i.e., $a_i = 0$. Note that $\Upsilon_{N_j}(a) = 1$ implies that $\|a\| \leq n - 2^{r-j}$. Therefore, there exists an assignment $a' \in A^j_k$ such that $a' \geq a$, $\|a'\| = \|a\| + 2^{r-j}$ and $a'_i = 1$. Then, we have $\Upsilon_{N_j}(a') = 0$ and $\Upsilon_{N_{j'}}(a') = \Upsilon_{N_{j'}}(a)$ for $j' \neq j$. By the monotonicity of Υ_H, we have $\Upsilon_H(a') \geq \Upsilon_H(a) = 1$. Thus, we have $1 = \Upsilon_G(a') \neq NEG^n_i(a') = 0$. ∎

By the duality of $\wedge$ and $\vee$, the following lemma is obtained.

Lemma 4.4.4 *$\Upsilon_H \vee \Upsilon_{N_j} = 1$ over A^j_k if G is an $\wedge$ gate.* ∎

From Lemma 4.4.3 and Lemma 4.4.4, we obtain the following lemma immediately.

Lemma 4.4.5 *$\Upsilon_{G'} = \Upsilon_{H'} = NEG^n_i$ over $A^{j-1}_{k'}$ for some $0 \leq k' < 2^{r-j+1}$.*

Proof. Note that $A^{j-1}_k = \{\, a \in A^j_k \mid \Upsilon_{N_j}(a) = 1 \,\}$ and $A^{j-1}_{k+2^{r-j}} = \{\, a \in A^j_k \mid \Upsilon_{N_j}(a) = 0 \,\}$. Thus, if G is an $\vee$ gate, from Lemma 4.4.3 $\Upsilon_{G'} = \Upsilon_{H'} = NEG^n_i$ over A^{j-1}_k. Otherwise, i.e., if G is an $\wedge$ gate, from Lemma 4.4.4, $\Upsilon_{G'} = \Upsilon_{H'} = NEG^n_i$ over $A^{j-1}_{k+2^{r-j}}$. ∎

From the definition of G', G' is in depth $D^0(T^n_{\lceil n/2 \rceil}) + 2j - 1$. Thus, from Lemma 4.4.5 and (i) and (ii) of Lemma 4.4.2, H' is in depth $D^0(T^n_{\lceil n/2 \rceil}) + 2j - 2$ if $j \geq 3$. Recall that Y_i is the i-th output gate, i.e., $\Upsilon_{Y_i} = NEG^n_i$ over $A^r_0 = \{0,1\}^n$.

Lemma 4.4.6 *For each $1 \leq i \leq n$, there exists a path to Y_i, which contains $2r-1$ gates such that*

(i) *for each $2 \leq j \leq 2r-1$, the j-th gate on such a path is in depth $D^0(T^n_{\lceil n/2 \rceil}) + j + 1$;*

(ii) *for each $1 \leq j < r$ and the $(2j-1)$-th and the $2j$-th gates on such a path compute NEG^n_i over A^j_k for some $0 \leq k < 2^{r-j}$.*

Proof. For each $1 \leq i \leq n$, start with a path with one gate, Y_i, in depth $D^0(T^n_{\lceil n/2 \rceil}) + 2r$, where $\Upsilon_{Y_i} = NEG^n_i$ over $A^r_0 = \{0,1\}^n$. From Lemma 4.4.2 and Lemma 4.4.5, such a path can be extended to a path which contains $2r-1$ gates as follow.

For $j = r, \ldots, 2$, let G be a gate in depth $D^0(T^n_{\lceil n/2 \rceil}) + 2j$ such that G is the source of such a path and $\Upsilon_G = NEG^n_i$ on A^j_k for some $0 \leq k < 2^{r-j}$. From Lemma 4.4.5, there exist a predecessor G' of G and a predecessor H' of G', such that $\Upsilon_{G'} = \Upsilon_{H'} = NEG^n_j$ over $A^{j-1}_{k'}$ for some $0 \leq k' < 2^{r-j+1}$. Then, we extend the path by adding 2 gates, G' and H'. G' is in depth $D^0(T^n_{\lceil n/2 \rceil}) + 2j - 1$, and from (ii) of Lemma 4.4.2 H' is in depth $D^0(T^n_{\lceil n/2 \rceil}) + 2j - 2$ for $j \geq 3$. In the last extension, i.e., $j = 2$, a gate G in in depth $D^0(T^n_{\lceil n/2 \rceil}) + 3$ and a gate H which is a predecessor of G are found. Since there exists a path from N_1 to H ($\Upsilon_H(x)$ is not a monotone function of x), H is in depth $D^0(T^n_{\lceil n/2 \rceil}) + 1$ or $D^0(T^n_{\lceil n/2 \rceil}) + 2$.

In each extension, 2 gates are added in the path. After $r-1$ extension, we obtain a path to Y_i which contains $2r-1$ gates. It can be verified easily that such a path satisfies the lemma. ∎

Let P_i be the path to Y_i found in this lemma, and let $G^i_1, G^i_2, \ldots, G^i_{2r-1}$ be the gates on P_i, such that G^i_j is the j-th gate on P_i, i.e., G^i_1 is in depth $D^0(T^n_{\lceil n/2 \rceil}) + 1$ or $D^0(T^n_{\lceil n/2 \rceil}) + 2$ and G^i_j is in depth $D^0(T^n_{\lceil n/2 \rceil}) + j + 1$ for $2 \leq j \leq 2r-1$.

Lemma 4.4.7 *$P_1, \ldots, P_n$ are disjoint.*

Proof. Suppose P_i and $P_{i'}$ share a gate G. Note that P_i and $P_{i'}$ must share G at the same position, i.e., $j = j'$ if $G = G^i_j = G^{i'}_{j'}$, since G^i_j and $G^{i'}_{j'}$ are in different depth if $j \neq j'$.

Suppose $G = G^i_{2j-1} = G^{i'}_{2j-1}$ (or $G = G^i_{2j} = G^{i'}_{2j}$) for some $1 \leq j \leq r$. Then, for some $0 \leq k, k' < 2^{r-j}$, $\Upsilon_G = NEG^n_i$ over A^j_k, and $\Upsilon_G = NEG^n_{i'}$ over $A^j_{k'}$. We have $k \neq k'$, since there exists an assignment $a \in A^j_k$ such that $a_i \neq a_{i'}$, i.e., $NEG^n_i(a) \neq NEG^n_{i'}(a)$. Assume without loss of generality that $k < k'$. Let $a \in A^j_k$ and $a' \in A^j_{k'}$ such that $a \leq a'$, $\|a\| = k$ with $a_i = 0$ and $a_{i'} = 1$, $\|a'\| = k'$ with $a'_i = 1$ and $a'_{i'} = 1$. Then, we have $\Upsilon_G(a) = NEG^n_i(a) = 1$. Note that Υ_G is a monotone function of x and all $N_{j'}$ for $j' < j$, and $\Upsilon_{N_{j'}}(a') = \Upsilon_{N_{j'}}(a) = 1$ for all $j' < j$ (since $k < k' < 2^{r-j}$). Thus, from the monotonicty of Υ_G we have $\Upsilon_G(a') \geq \Upsilon_G(a) = 1$. However, it contradicts to the assumption, $\Upsilon_G = NEG^n_{i'}$ over $A^j_{k'}$, since $1 = \Upsilon_G(a') \neq NEG^n_{i'}(a') = 0$ for some $a' \in A^j_{k'}$. ∎

Now, we are now ready to prove Theorem 4.4.1.

Proof of Theorem 4.4.1. From Lemma 4.4.6 and Lemma 4.4.7, $n(2r-1)$ gates are found in depth greater than $D^0(T^n_{\lceil n/2 \rceil})$. Furthermore, $\Upsilon_{Z_1} = T^n_{\lceil n/2 \rceil}$ is computed at the predecessor Z_1 of N_1. Thus, there are at least $4n - O(1)$ gates in depth not greater than $D^0(T^n_{\lceil n/2 \rceil})$, since $C^0(T^n_{\lceil n/2 \rceil}) \geq 4n - O(1)$ (see [5, 10]). ∎

4.5 Conclusion

We consider both the depth and size of negation-limited inverters. For the depth of negation-limited inverters, we have improved the upper bounds from the previous result [4] by a factor of 3. Since minimum depth of monotone circuits computing threshold functions are not precise, we do not know whether our upper bound matches the lower bound or not. However it is conjectured that the threshold function $T^n_{\lceil n/2 \rceil}$ is the most difficult threshold function, i.e.,

$$D^0(T^n_{\lceil n/2 \rceil}) = D^0(T^n_1, \ldots, T^n_n)\,.$$

For the size of negation-limited inverters, we have shown by using the result shown in chapter 3, a $7.33n$ lower bound on size of negation-limited inverters, which improve the

lower bound from the previous result shown by Tanaka and Nishino [18] more than $2n$. However, the best upper bound on size of negation-limited inverters is $O(n \log n)$ [4], and it is conjectured that the minimum size of negation-limited inverters is $\Omega(n \log n)$.

While proving $\Omega(n \log n)$ lower bound on size of negation-limited inverters remains a very hard open problem, by assuming that our upper bound on depth matches the lower bound of that, i.e.,

$$D^0(T^n_{\lceil n/2 \rceil}) = D^0(T^n_1, \ldots, T^n_n)\,.$$

we have shown a $2n \log n + 3n$ lower bound on size of minimum depth negation-limited inverters over basis $\{\wedge, \vee, \overline{\wedge}, \overline{\vee}\}$.

It is not certain whether our technique is useful for proving lower bound on size of negation-limited inverters. Note that most of the gates that we find in the lower bound are above the first negation gate N_1 (i.e., in the non-monotone subcircuit). It seems there are also $\Omega(n \log n)$ of gates below N_1 (i.e., in the monotone subcircuit).

Chapter 5

Minimum number of negations in threshold circuits

5.1 Previous works

Markov [11] showed the minimum number of negation gates in circuits computing an arbitrary collection of Boolean functions F, i.e., the inversion complexity $I(F)$.

$$I(F) = \lceil \log(d(F) + 1) \rceil$$

On the other hand, Santha and Wilson [14] showed that in the case of unbounded fan-in circuits, including threshold circuits, $I(F)$ negation gates are not sufficient to compute F if the depth of circuits is small (e.g., constant). They showed a lower bound of the minimum number of negation gates in constant depth circuits as a trade-off of depth and the number of negation gates. Precisely, a depth D threshold circuit computing an arbitrary collection of Boolean functions F require at least

$$D(d(F) + 1)^{1/D} - D$$

negation gates. Note that the lower bound tends to 0 when D grows. Thus, for some sufficiently large D, the lower bound is less than the inversion complexity $I(F)$, i.e., it is not *tight*.

They also constructed a depth $2D+O(1)$ threshold circuit computing NEG^n consisting of $Dd(NEG^n)^{1/D} - D + 1$ negation gates for any $D \geq 1$.

In this chapter, we show that their lower bound can be slightly improved, so that the lower bound showed by Markov [11] can be obtain as a special case of our lower bound. We also show that there exists a threshold circuit computing a collection of Boolean functions such that the number of negation gates in it matches our lower bound.

5.1.1 Result of Santha and Wilson

We first briefly explain the lower bound showed by Santha and Wilson [14]. Let F be an arbitrary collection of Boolean functions. We rewrite their proof in terms of $d(F)$.

Theorem 5.1.1 (Santha and Wilson [14]) *Any depth D threshold circuit computing F contains at least $D(d(F)+1)^{1/D} - D$ negation gates.*

Note that the lower bound $D(d(F)+1)^{1/D} - D$ tends to 0 when D grows. Before proving Theorem 5.1.1, we show some relations between decreases and gates in circuits. Let α be an arbitrary chain. Then we have the following lemmas.

Lemma 5.1.2 *Suppose G is a monotone gate with predecessor $G_1, \ldots, G_m$. Then,*

$$dec(\Upsilon_G, \alpha) \subseteq \bigcup_{j=1}^{m} dec(\Upsilon_{G_j}, \alpha)\,.$$

Proof. Suppose $i \in dec(\Upsilon_G, \alpha)$ and $i \notin \bigcup_{j=1}^{m} dec(\Upsilon_{G_j}, \alpha)$ for some $0 \leq i < n$. It implies that $i \notin dec(\Upsilon_{G_j}, \alpha)$ for $1 \leq j \leq m$, i.e., $\Upsilon_{G_j}(\alpha^{i-1}) \leq \Upsilon_{G_j}(\alpha^i)$. From the monotonicity of Υ_G, we have $\Upsilon_G(\alpha^{i-1}) \leq \Upsilon_G(\alpha^i)$, i.e., $i \notin dec(\Upsilon_G, \alpha)$. ∎

Lemma 5.1.3 *Suppose G is an negation gate with predecessors $G_1, \ldots, G_m$. Then,*

$$|dec(\Upsilon_G, \alpha)| \leq \sum_{i=1}^{m} \left|dec(\Upsilon_{G_i}, \alpha)\right| + 1\,.$$

Proof. Since G is an negation gate, $\neg\Upsilon_G$ is a monotone function of Υ_{G_i} for $1 \leq i \leq m$. From Lemma 5.1.2, $dec(\neg\Upsilon_G, \alpha) \subseteq \bigcup_{i=1}^{m} dec(\Upsilon_{G_i}, \alpha)$, i.e.,

$$|dec(\neg\Upsilon_G, \alpha)| \leq \sum_{i=1}^{m} \left|dec(\Upsilon_{G_i}, \alpha)\right|.$$

Suppose $|dec(\neg\Upsilon_G, \alpha)| = k$ and the satisfying set $S(\neg\Upsilon_G, \alpha)$ of $\neg\Upsilon_G$ over α can be represented as follows.

$$S(\neg\Upsilon_G, \alpha) = [l_1, l_2) \cup [l_3, l_4) \cup \cdots \cup [l_{2k-1}, l_{2k}) \cup [l_{2k+1}, n+1)\,,$$

where $0 \leq l_1 < l_2 < \cdots < l_{2k+1} \leq n+1$ and $dec(\neg\Upsilon_G, \alpha) = \{\, l_2, l_4, \ldots, l_{2k} \,\}$. Then, we have

$$S(\Upsilon_G, \alpha) = [0, l_1) \cup [l_2, l_3) \cup \cdots \cup [l_{2k}, l_{2k+1})\,,$$

and $dec(\Upsilon_G, \alpha) \subseteq \{\, l_1, l_3, \ldots, l_{2k+1} \,\}$. It implies that $|dec(\Upsilon_G, \alpha)| \leq k+1$. ■

Note that from this lemma, $|dec(\Upsilon_G, \alpha)| = k+1$ if and only if $l_1 > 0$ and $l_{2k+1} < n+1$.

Proof of Theorem 5.1.1. Let C be a depth D threshold circuit computing F, and let ν_i for $1 \leq i \leq D$ be the number of negation gates at level i in C, i.e., C consists of $\nu = \sum_{i=1}^{D} \nu_i$ negation gates. We show the upper bound on the number of decreases which can be created in C, and such an upper bound is not less than $d(F)$.

Level 0 consists of inputs, $x_1, \ldots, x_n$, where $dec(x_i, \alpha) = \emptyset$ for all $1 \leq i \leq n$, i.e., no decrease is created at level 0. Suppose $k-1 \geq 0$ decreases are created by gates in level i' for all $1 \leq i' < i$. From Lemma 5.1.2 and 5.1.3, only negation gates can create decreases, and each negation gate in level i can create at most k decreases. Thus, in level i there are at most $k\nu_i$ new decreases are created, and totally there are at most $k(1+\nu_i) - 1$ decreases are created by gates in level i' for all $0 \leq i' \leq i$. Thus, the circuit can create at most $\prod_{i=1}^{D}(1+\nu_i) - 1$ decreases. Therefore, we must have

$$\prod_{i=1}^{D}(1+\nu_i) - 1 \geq d(F)\,. \tag{5.1}$$

The product $\prod_{i=1}^{D}(1+\nu_i)$ is maximized when $\nu_i = \nu/D$, it follows that

$$\nu \geq D(d(F)+1)^{1/D} - D\,.$$

■

5.2 Lower bounds

We show that the result of Santha and Wilson can be slightly improved. Since $\nu_1, \ldots, \nu_D$ in Theorem 5.1.1 are *integers*, the lower bound of the number of negation gates in a depth D threshold circuit computing F can be precisely represented as follows.

$$\min \left\{ \sum_{i=1}^{D} \nu_i \;\middle|\; \nu_1, \ldots, \nu_D \in \mathbf{N},\ \prod_{i=1}^{D} (1+\nu_i) \geq d(F)+1 \right\} . \tag{5.2}$$

For positive integers ν, D and w let $\pi : \mathbf{N} \times \mathbf{N} \to \mathbf{N}$ be a function defined as

$$\pi(\nu, D) = \max \left\{ \prod_{i=1}^{D} (1+\nu_i) \;\middle|\; \nu_1, \ldots, \nu_D \in \mathbf{N},\ \sum_{i=1}^{D} \nu_i = \nu \right\} ,$$

and let

$$\sigma(w, D) = \min\{\, \nu \mid \pi(\nu, D) \geq w+1 \,\} .$$

Then, the solution of (5.2) is $\sigma(d(F), D)$. We have the following Theorem.

Theorem 5.2.1 *Any depth D threshold circuit computing F contains at least $\sigma(d(F), D)$ negation gates.*

In the following, we show precisely the value of $\pi(\nu, D)$ and $\sigma(w, D)$.

Lemma 5.2.2 $\pi(\nu, D) = (1 + \lceil \nu/D \rceil)^k (1 + \lfloor \nu/D \rfloor)^{D-k}$ *for some* $0 \leq k \leq D$.

Proof. Suppose $\pi(\nu, D) = \prod_{i=1}^{D} (1+\nu_i)$ where $\nu_1, \ldots, \nu_i$ are non-negative integers satisfying $\sum_{i=1}^{D} \nu_i = \nu$. It is sufficient to show that $\nu_i \in \{\, \lfloor \nu/D \rfloor, \lceil \nu/D \rceil \,\}$ for $1 \leq i \leq D$. First, we show that $\nu_1, \ldots, \nu_D$ satisfy

$$\max\{\, \nu_1, \ldots, \nu_D \,\} - \min\{\, \nu_1, \ldots, \nu_D \,\} \leq 1 . \tag{5.3}$$

Suppose there exist $1 \leq j, j' \leq D$ such that $\nu_j - \nu_{j'} > 1$. Then, there exist D non-negative integers $\hat{\nu}_1, \ldots, \hat{\nu}_D$ such that

$$\hat{\nu}_i = \begin{cases} \nu_i - 1 & \text{if } i = j, \\ \nu_i + 1 & \text{if } i = j', \\ \nu_i & \text{otherwise.} \end{cases}$$

It is obvious that $\sum_{i=1}^{D} \hat{\nu}_i = \nu$. Since $\nu_j - \nu_{j'} > 1$, we have

$$\begin{aligned}(1+\hat{\nu}_j)(1+\hat{\nu}_{j'}) &= (1+\nu_j)(1+\nu_{j'}) + \nu_j - \nu_{j'} - 1 \\ &> (1+\nu_j)(1+\nu_{j'})\end{aligned}$$

and thus

$$\begin{aligned}\prod_{i=1}^{D}(1+\hat{\nu}_i) &= \frac{(1+\hat{\nu}_j)(1+\hat{\nu}_{j'})}{(1+\nu_j)(1+\nu_{j'})} \prod_{i=1}^{D}(1+\nu_i) \\ &> \prod_{i=1}^{D}(1+\nu_i)\,.\end{aligned}$$

It contradicts to the maximality of $\pi(\nu, D)$. Therefore, $\nu_1, \ldots, \nu_D$ satisfy (5.3).

Then, we show that

$$\lfloor \nu/D \rfloor \leq \min\{\, \nu_1, \ldots, \nu_D \,\} \leq \max\{\, \nu_1, \ldots, \nu_D \,\} \leq \lceil \nu/D \rceil\,. \tag{5.4}$$

If $\min\{\, \nu_1, \ldots, \nu_D \,\} < \lfloor \nu/D \rfloor$, then from (5.3) we have $\max\{\, \nu_1, \ldots, \nu_D \,\} \leq \lfloor \nu/D \rfloor$, and thus

$$\sum_{i=1}^{D} \nu_i \leq D\lfloor \nu/D \rfloor - 1 < \nu\,.$$

If $\max\{\, \nu_1, \ldots, \nu_D \,\} > \lceil \nu/D \rceil$, then from (5.3) $\min\{\, \nu_1, \ldots, \nu_D \,\} \geq \lceil \nu/D \rceil$, and thus

$$\sum_{i=1}^{D} \nu_i \geq D\lceil \nu/D \rceil + 1 > \nu\,.$$

It follows that $\pi(\nu, D) = (1 + \lceil \nu/D \rceil)^k (1 + \lfloor \nu/D \rfloor)^{D-k}$ for some integer $0 \leq k \leq D$. ∎

Lemma 5.2.3 *Let w and D be arbitrary positive integers. Then*

$$\sigma(w, D) = k\lceil (w+1)^{1/D} \rceil + (D-k)\lfloor (w+1)^{1/D} \rfloor - D\,,$$

for the smallest non-negation integer k such that

$$\lceil (w+1)^{1/D} \rceil^k \lfloor (w+1)^{1/D} \rfloor^{D-k} \geq w+1\,.$$

Proof. Let ν be the smallest integer satisfies $\pi(\nu, D) \geq w+1$, i.e., $\nu = \sigma(w, D)$. From Lemma 5.2.2, we have

$$\pi(\nu, D) = (1 + \lceil \nu/D \rceil)^k (1 + \lfloor \nu/D \rfloor)^{D-k} \geq w\,.$$

for some $0 \leq k \leq D$. First, we show that

$$\lfloor (w+1)^{1/D} \rfloor - 1 \leq \lfloor \nu/D \rfloor \leq \lceil \nu/D \rceil \leq \lceil (w+1)^{1/D} \rceil - 1 \,.$$

If $\lceil \nu/D \rceil < \lfloor (w+1)^{1/D} \rfloor - 1$, then

$$\pi(\nu, D) \leq (1 + \lceil \nu/D \rceil)^D < \lfloor (w+1)^{1/D} \rfloor^D \leq w+1 \,.$$

If $\lfloor \nu/D \rfloor > \lceil (w+1)^{1/D} \rceil - 1$, then

$$\lfloor (\nu-1)/D \rfloor \geq (1 + \lfloor \nu/D \rfloor)^D > \lceil (w+1)^{1/D} \rceil^D \,.$$

It implies that $\pi(\nu - 1, D) > \lceil (w+1)^{1/D} \rceil^D \geq w+1$, and it contradicts to the minimality of ν. Thus we have

$$\pi(\nu, D) = \lceil (w+1)^{1/D} \rceil^k \lfloor (w+1)^{1/D} \rfloor^{D-k} \,,$$

with $\nu = k\lceil (w+1)^{1-D} \rceil + (D-k)\lfloor (w+1)^{1/D} \rfloor - D$ for some integer $0 \leq k \leq D$. From the minimality of ν, k is the smallest non-negation integer such that

$$\lceil (w+1)^{1/D} \rceil^k \lfloor (w+1)^{1/D} \rfloor^{D-k} \geq w+1 \,.$$

■

Thus, we can obtain the lower bound of minimum number of negation gates in a circuit computing F as Theorem 3.1.1. That is,

$$\min_D \{ \, \sigma(d(F), D) \, \} = \lceil \log(d(F)+1) \rceil \,.$$

Since we have $\lceil (d(F)+1)^{1/D} \rceil = 2$ if $d(F) \geq 1$ and $D \geq \lceil \log(d(F)+1) \rceil$. It implies that $\sigma(d(F), D) = \lceil \log(d(F)+1) \rceil$.

5.3 Upper bounds

In this section, we show that for some collections of Boolean functions F, there exist threshold circuits computing F each of which contains at most $\sigma(d(F), D)$ negation gates as shown in Theorem 5.2.1.

Let $F_M = (f_1, \ldots, f_{M-1})$ for $M \geq 2$ be a collection of Boolean functions such that for each $1 \leq j \leq M-1$,

$$f_j(x) = 1 \quad \text{iff} \quad \|x\| \bmod M < j\,.$$

First, we construct a depth 2 threshold for F_M. For arbitrary positive integers M_1 and M_2 satisfying $M_1 M_2 > n$, we define $H^i = (h_1^i, \ldots, h_{M_i-1}^i)$ for $i = 1, 2$ as follows. For $1 \leq j \leq M_1 - 1$,

$$h_j^1(x) = 1 \quad \text{iff} \quad \|x\| \bmod M_1 M_2 < jM_2\,.$$

and for $1 \leq j \leq M_2 - 1$,

$$h_j^2(x) = 1 \quad \text{iff} \quad \|x\| \bmod M_2 < j\,.$$

Thus, if $M_2 = M$, $F_M = H^2$, i.e., $f_j = h_j^2$ for each $1 \leq j \leq M_2 - 1$.

Since $M_1 M_2 \geq n+1$, h_j^1 is negation of a threshold function of x, i.e.,

$$h_j^1(x) = 1 \quad \text{iff} \quad \|x\| < jM_2\,.$$

Then, we have

$$\|H^1(x)\| = k \quad \text{iff} \quad (M_1 - k - 1)M_2 \leq \|x\| < (M_1 - k)M_2\,.$$

It implies that $M_1 M_2 - M_2 \leq \|x\| + M_2\|H^1(x)\| < M_1 M_2$, i.e.,

$$0 \leq \|x\| + M_2\|H^1(x)\| - (M_1 M_2 - M_2) < M_2\,.$$

We can represent $\|x\| \bmod M_2$ as follows.

$$\|x\| \bmod M_2 = \|x\| + M_2\|H^1(x)\| - (M_1 M_2 - M_2)\,.$$

Thus, h_j^2 is negation of a threshold function of x and H^1, i.e.,

$$h_j^2(x) = 1 \quad \text{iff} \quad \|x\| + M_2\|H^1(x)\| < (M_1 M_2 - M_2) + j\,.$$

Thus, we have the following theorem.

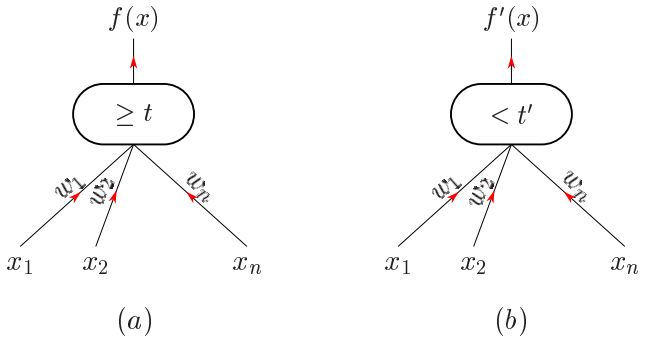

Figure 5.1: Threshold gates: (a) a monotone gate computes $f(x) = 1$ if and only if $\sum_{i=1}^{n} w_i x_i \geq t$, (b) a negation gate computes $f'(x) = 1$ if and only if $\sum_{i=1}^{n} w_i x_i < t'$.

Theorem 5.3.1 *For arbitrary positive integers M_1 and M_2 satisfying $M_1 M_2 \geq n+1$ and $M_2 \geq 2$, there exists a depth 2 threshold circuit computing F_{M_2} which consists of $M_1 + M_2 - 2$ negation gates.*

Proof. From the above argument, each h_j^1 is negation of a threshold function of x, and each h_j^2 is negation of a threshold function of x and H^1. We can compute the H^1 in depth 1 by using $M_1 - 1$ negation gates. Then, given the H^1 we can compute the H^2 $(= F_{M_2})$ in depth 1 by using $M_2 - 1$ negation gates. ∎

This theorem can be generalized to constructed any depth $D > 2$ threshold circuit computing F_M for $M \geq 2$.

Theorem 5.3.2 *For arbitrary positive integers $M_1, \ldots, M_D$ satisfying $M_1 \cdots M_D \geq n+1$ and $M_D \geq 2$, there exists a depth D threshold circuit computing F_{M_D} which consists of $\sum_{i=1}^{D} M_i - D$ negation gates.*

Proof. First, let us define collections of Boolean functions $H^i = (h_1^i, \ldots, h_{M_i-1}^i)$ for $1 \leq i \leq D$. For $1 \leq j \leq M_i - 1$,

$$h_j^i(x) = 1 \quad \text{iff} \quad \|x\| \bmod N_i < jN_{i+1}\,,$$

where $N_i = \prod_{j=i}^{D} M_j$ for $1 \leq i \leq D$ and $N_{D+1} = 1$.

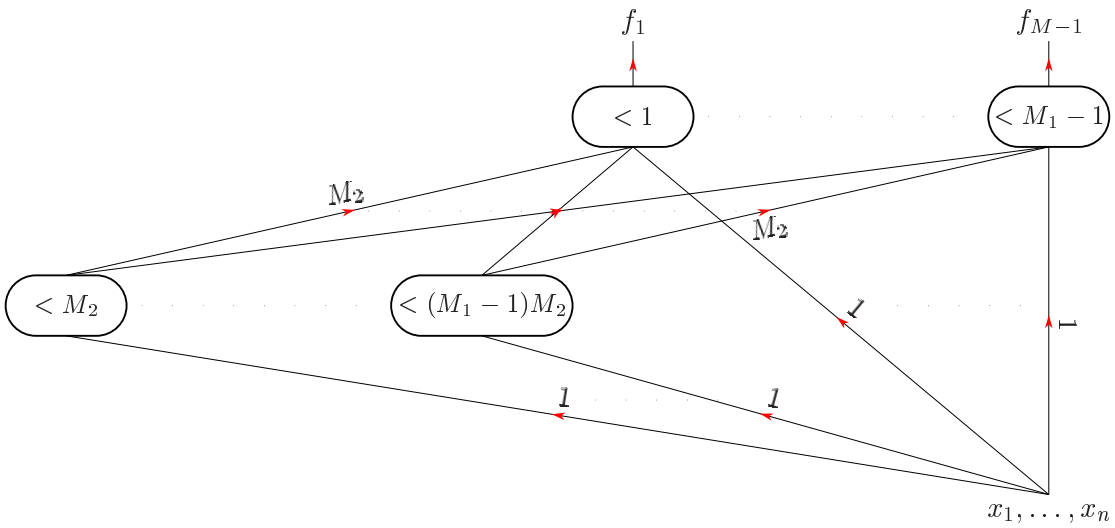

Figure 5.2: A depth 2 threshold circuit computing $F_M = (f_1, \ldots, f_{M-1})$.

Again, since $N_1 > n$, h_j^1 is negation of a threshold function of x, i.e.,

$$h_j^1(x) = 1 \quad \text{iff} \quad \|x\| < jN_2 \,.$$

Then we show that h_j^i for $1 < i \leq D$ is negation of a threshold function of x and the H^k for $1 \leq k \leq i-1$ by proving the following claim.

Claim: For $1 \leq i \leq D$,

$$\|x\| \bmod N_i = \|x\| + \sum_{k=1}^{i-1} N_{k+1} \|H^k(x)\| - (N_1 - N_i) \,.$$

Proof of Claim. Since $\left(\sum_{k=1}^{i-1} N_{k+1}\|H^k(x)\| - (N_1 - N_i)\right) \bmod N_i = 0$, we have

$$\|x\| \equiv \|x\| + \sum_{k=1}^{i-1} N_{k+1} \|H^k(x)\| - (N_1 - N_i) \pmod{N_i} \,.$$

Then, we prove by induction on i that

$$N_1 - N_i \leq \|x\| + \sum_{k=1}^{i-1} N_{k+1} \|H^k(x)\| < N_1$$

Base: It is clear for $i = 1$.

Induction: Suppose the claim is satisfied for some $1 \leq i \leq D$. Since

$$\|H^i(x)\| = j \quad \text{iff} \quad (M_i - j - 1)N_{i+1} \leq \|x\| \bmod N_i < (M_i - j)N_{i+1}\,,$$

we have by the induction hypothesis, $\|H^i(x)\| = j$ iff

$$N_1 - N_i + (M_i - j - 1)N_{i+1} \leq \|x\| + \sum_{k=1}^{i-1} N_{k+1}\|H^k(x)\| < N_1 - jN_{i+1}\,.$$

Thus, we have $N_1 - N_{i+1} \leq \|x\| + \sum_{k=1}^{i} N_{k+1}\|H^k(x)\| < N_1$. ∎

Thus, each h_j^i for $1 < i \leq D$ and $1 \leq j \leq M_i - 1$ is negation of a threshold function of x and the H^k for $1 \leq k \leq i-1$, i.e.,

$$h_j^i(x) = 1 \quad \text{iff} \quad \|x\| + \sum_{k=1}^{i-1} N_{k+1}\|H^k(x)\| < N_1 - N_i + jN_{i+1}\,.$$

From the above argument, the H^1 can be computed in depth 1 by using $M_1 - 1$ negation gates, and the H^i for $1 < i \leq D$ can be computed in depth 1 by using $M_i - 1$ negation gates if the H^k for $1 \leq k < i$ are given. Thus, we can construct a depth D threshold circuit computing $H^D = F_{M_D}$ which has size $\sum_{i=1}^{D} M_i - D$. ∎

Let $F'_M = (f_0, \ldots, f_{M-1})$ be a collection of M Boolean functions defined as follows.

$$f_0(x) = 1 \quad \text{iff} \quad \|x\| \bmod M \geq 1\,,$$

and $(f_1, \ldots, f_{M-1}) = F_M$.

Lemma 5.3.3 *For any M and n, $d(F'_M) = n$.*

Proof. It is sufficient to show that $dec(F'_M, \alpha) = \{1, \ldots, n\}$ for some chain α. Let α be an arbitrary chain. Since $f_j(\alpha^{i-1}) = 1$ and $f_j(\alpha^i) = 0$ if $i \bmod M = j$, for $0 \leq j \leq M-1$ and for $1 \leq i \leq n$, we have for $0 \leq j \leq M-1$

$$dec(f_j, \alpha) = \{\, i \mid 1 \leq i \leq n,\, i \bmod M = j \,\}\,.$$

Thus, we have

$$dec(F'_M, \alpha) = \bigcup_{j=0}^{M-1} dec(f_j, \alpha) = \bigcup_{j=0}^{M-1} \{\, i \mid 1 \leq i \leq n,\, i \bmod M = j \,\} = \{\, 1, \ldots, n \,\}.$$

∎

Theorem 5.3.4 *For arbitrary positive integers $M_1, \ldots, M_D$ satisfying $M_1 \cdots M_D \geq n+1$ and $M_D \geq 2$, there exists a depth D threshold circuit computing F'_{M_D} which consists of $\sum_{i=1}^{D} M_i - D$ negation gates and one monotone gate.*

Proof. First, from Theorem 5.3.2, we can construct a depth D threshold circuit computing F_{M_D} which has size at most $\sum_{i=1}^{D} M_i - D$. Then, since

$$\|x\| \bmod N_D = \|x\| + \sum_{k=1}^{D-1} N_{k+1}\|H^k(x)\| - (N_1 - N_D)\,.$$

f_0 is a threshold function of x and the H^k for $1 \leq k \leq D-1$, i.e.,

$$f_0(x) = 1 \quad \text{iff} \quad \|x\| + \sum_{k=1}^{D-1} N_{k+1}\|H^k(x)\| \geq N_1 - N_D + 1\,.$$

Thus, f_0 can be computed in parallel with f_j for $1 \leq j < M$ by using a monotone gate. ■

Let k be the smallest index such that

$$\lceil (n+1)^{1/D} \rceil^k \lfloor (n+1)^{1/D} \rfloor^{D-k} \geq n+1\,.$$

Then, from Theorem 5.3.4, by putting $M_1 = \cdots = M_k = \lceil (n+1)^{1/D} \rceil$ and $M_{k+1} = \cdots = M_D = \lfloor (n+1)^{1/D} \rfloor$, we can obtain a depth D threshold circuit computing F_{M_D} which consists of

$$\sum_{i=1}^{D} M_i - D = \lfloor (n+1)^{1/D} \rfloor + k - D = \sigma(n, D) = \sigma(d(F_{M_D}), D)$$

negation gates and one monotone gate. Therefore, the number of negation gates in such a threshold circuit matches the lower bound shown in Theorem 5.2.1.

5.4 Conclusion

We have slightly improved the previous lower bound [14] on the minimum number of negation gates in threshold circuits. We have also shown that for some collection of Boolean functions F_M such that there exists a depth D threshold circuit computing F_M which contains minimum number of negation gates. That is, the number of negation gates

in such a threshold circuit matches our lower bound. It implies that our lower bound is a *tight* bound.

However, for some Boolean functions, the lower bound on minimum number of negation gates can be improved (See Chapter 6). It means that the lower bound on minimum number of negation gates should be proved not only in terms of $d(F)$ of a given collection of Boolean function F.

For other unbounded fan-in circuits such as AC circuits, i.e., circuits with basis $\{\wedge, \vee, \neg\}$ with $\wedge$ and $\vee$ of arbitrary number of variables, we do not know much of the minimum number of negation gates in AC circuits computing an arbitrary Boolean function (See [14]).

Chapter 6

Negation-limited threshold circuits

6.1 Previous works

The first explicit construction of negation-limited threshold circuit computing NEG^n was presented by Akers [2]. His circuit uses $\lceil \log(n+1) \rceil$ negation gates, and has size $n + \lceil \log(n+1) \rceil$ and depth $\lceil \log(n+1) \rceil + 1$. Recently, Santha and Wilson [14] showed a negation-limited threshold circuit computing NEG^n of depth $2D + O(1)$ using $D(n+1)^{1/D} - D + 1$ negation gates.

Threshold circuits computing $PARITY^n$ has been investigated by Impagliazzo, Paturi and Saks [9], Sung and Nishino [16] and Wegener [21]. Wegener [21] showed that $PARITY^n$ can be computed by a threshold circuit with size $\lceil \log(n+1) \rceil$ and depth $\lceil \log(n+1) \rceil$. It is shown that such a threshold circuit has minimum size. He also showed a lower bound on size of threshold circuits computing an arbitrary Boolean function. He posed the following open problem.

> **Open problem:** *Determine the minimum depth such that the parity function have circuits of polylogarithmic, i.e.,* $\log^{O(1)} n$*, size.*

6.2 Negation-limited Inverters

We called a threshold circuit computing NEG^n which contains minimum number of negation gates, a *negation-limited inverter*. In this section, we show the *number of negation gates* in depth D negation-limited inverters, minimum number of negation gates in depth

D threshold circuits computing NEG^n. Furthermore, we show the *minimum size* of negation-limited inverters.

6.2.1 Number of negations

First, we show the *upper bound* on the number of negation gates in negation-limited inverters.

Lemma 6.2.1 *For arbitrary positive integers $M_1, \ldots, M_D$ satisfying $M_1 \cdots M_D \geq n+1$ and $M_D \geq 2$, there exists a depth $D+1$ threshold circuit computing NEG^n which consists of $\sum_{i=1}^{D} M_i - D$ negation gates and n monotone gates.*

Proof. First, from Theorem 5.3.2, a depth D threshold circuit computing F_{M_D} which has size $\sum_{i=1}^{D} M_i - D$ is constructed. From the claim in Theorem 5.3.2, we have

$$\|x\| + \sum_{k=1}^{D} N_{k+1}\|H^k(x)\| - (N_1 - 1) = 0\,.$$

It implies that $NEG_i^n(x) = \neg x_i$ is a threshold function of x and H^i for $1 \leq i \leq D$, i.e.,

$$NEG_i^n(x) = 1 \quad \text{iff} \quad \|x\| - x_i + \sum_{k=1}^{D} N_{k+1}\|H^k(x)\| \geq N_1 - 1\,.$$

Note that the term $\|x\| - x_i$ is $\sum_{j=1}^{i-1} x_j + \sum_{j=i+1}^{n} x_j$. We can compute NEG^n in depth 1 by using n monotone gates if the H^i for $1 \leq i \leq D$ are given. Therefore, we can construct a depth $D+1$ threshold circuits computing NEG^n which consists of $\sum_{i=1}^{D} M_i - D$ negation gates and n monotone gates. ∎

From this theorem, for the smallest k such that

$$\lceil (n+1)^{1/D} \rceil^k \lfloor (n+1)^{1/D} \rfloor^{D-k} \geq n+1 = d(NEG^n) + 1\,,$$

by putting $M_1 = \cdots = M_k = \lceil (n+1)^{1/D} \rceil$ and $M_{k+1} = \cdots = M_D = \lfloor (n+1)^{1/D} \rfloor$, we obtain a depth $D+1$ threshold circuit computing NEG^n which contains

$$\begin{aligned} \sum_{i=1}^{D} M_i - D &= k\lceil (n+1)^{1/D} \rceil + (D-k)\lfloor (n+1)^{1/D} \rfloor - D \\ &= \sigma(n, D) \\ &= \sigma(d(NEG^n), D) \end{aligned}$$

negation gates.

Theorem 6.2.2 *Any depth $D+1$ negation-limited inverter contains at most $\sigma(n, D)$ negation gates.*

Note that by the same argument, we obtain a $\sigma(n, D) + n$ upper bound on size of depth D negation-limited inverters.

Then, we show the *lower bound* on the number of negation gates in negation-limited inverters. It is obvious (from Theorem 5.2.1) that any depth 1 negation-limited inverter contains at least $n = \sigma(n, 1)$ negation gates. In the following, we show that depth $D+1$ (≥ 2) threshold circuits computing NEG^n require $\sigma(n, D)$ negation gates.

Theorem 6.2.3 *Any depth $D+1$ (≥ 2) negation-limited inverter contains at least $\sigma(n, D)$ negation gates.*

Proof. Suppose an arbitrary depth $D+1$ negation-limited inverter C is given, where C contains ν negation gates. We can assume without loss of generality that all gates in level $D+1$ are output gates. Otherwise, gates in level $D+1$ which are not output gates can be eliminated, and the resulting circuit is also a negation-limited inverter.

Then, if there exists a negation gate G in level $D+1$, then from the assumption such negation gates are output gates, i.e., $\Upsilon_G = NEG_i^n$ for some $1 \leq i \leq n$. Then, we can replace G by a negation gate G' computing $\neg x_i$ directly from x_i, and such a gate G' is in level 1. By such a way, we can obtain a depth $D+1$ negation-limited inverter C' such that the number of negation gates in C' is at most ν, and there is no negation gate in level $D+1$ of C'.

Let ν_j for $1 \leq j \leq D+1$ be the number of negation gates in level j of C'. Note that $\nu_{D+1} = 0$ and C' contains $\sum_{j=1}^{D+1} \nu_j$ negation gates, where $\sum_{j=1}^{D+1} \nu_j \leq \nu$. By the same argument of Theorem 5.2.1, we have

$$\sigma(n, D) \leq \sum_{j=1}^{D+1} \nu_j \leq \nu \,.$$

Therefore, C (and C') contains at least $\sigma(n, D)$ negation gates. ∎

From this theorem, any depth 2 threshold circuit computing NEG^n consists of at least $n = \sigma(n, 1)$ negation gates. Therefore, there is no advantage to construct depth 2 negation-limited inverters. From Theorem 6.2.2 and Theorem 6.2.3, we have the following corollary.

Corollary 6.2.4 *Any depth $D+1$ (> 2) negation-limited inverter contains exactly $\sigma(n, D)$ negation gates.*

6.2.2 Minimum size

In previous subsection, we obtain a $\sigma(n, D)+n$ upper bound on size of depth D negation-limited inverter. We show that this upper bound can be improved, and we also show a lower bound which matches the new upper bound.

For the case

$$\sigma(n, D) = \sigma(n-1, D) + 1\,,$$

there exists a depth $D+1$ negation-limited inverter with one gate less, i.e., such a negation-limited inverter contains $\sigma(n, D)+n-1$ gates. In such cases, we can compute $NEG_1^n(x) = \neg x_1$ by a negation gate directly from x_1, and compute $NEG_2^n(x), \ldots, NEG_n^n(x)$ by a depth $D+1$ negation-limited inverter of $x_2, \ldots, x_n$ with $\sigma(n-1, D) + n - 1$ gates. Totally, $\sigma(n, D) + n - 1$ gates, including exactly $\sigma(n, D)$ negation gates, are used. Thus, we have the following theorem.

Theorem 6.2.5 *There exists a depth $D+1$ negation-limited inverter whose size is $\sigma(n-1, D) + n$.*

Proof. From the above argument, it is sufficient to show that

$$\sigma(n-1, D) + n = \begin{cases} \sigma(n, D) + n - 1 & \text{if } \sigma(n, D) = \sigma(n-1, D) + 1, \\ \sigma(n, D) + n & \text{otherwise.} \end{cases} \tag{6.1}$$

Note that from the minimality and the monotonicity of $\sigma(n, D)$, we have

$$\sigma(n, D) - 1 \leq \sigma(n-1, D) \leq \sigma(n, D)\,,$$

and it implies (6.1). ∎

Then, we show that lower bound on *size* of depth D negation-limited inverters.

Lemma 6.2.6 *In any depth $D+1$ (>2) negation-limited inverter (with $n>2$), there is at most one negation output gate. In particular, $\sigma(n,D)=\sigma(n-1,D)+1$ if there exists a negation output gate.*

Proof. Suppose there exists a depth $D+1$ negation-limited inverter C such that one output gate G of C is a negation gate. Assume without loss of generality that $\Upsilon_G(x)=\neg x_1$. From Corollary 6.2.4, C contains $\nu=\sigma(n,D)$ negation gates. By replacing x_1 by 1 and G by 0, we obtain a depth $D'\leq D+1$ threshold circuit computing NEG^{n-1} which contains $\nu-1$ negation gates. It implies that $\nu-1$ negation gates are sufficient to compute NEG^{n-1} by a depth $D+1$ threshold circuit, i.e., $\pi(\nu-1,D)\geq n$. From the minimality of ν, we have $\pi(\nu-1,D)\leq n$. It implies that $\pi(\nu-1,D)=n$ and $\nu-1=\sigma(n-1,D)$. Therefore, $\sigma(n,D)=\sigma(n-1,D)+1$ if there exists a negation output gate.

Suppose C contains two negation output gates G and G'. Assume without loss of generality that $\Upsilon_G(x)=\neg x_1$ and $\Upsilon_{G'}(x)=\neg x_2$. By replacing x_1 and x_2 by 1, and, G and G' by 0, we obtain a depth $D''\leq D+1$ threshold circuit computing NEG^{n-2} which contains $\nu-2$ negation gates. It implies that $\nu-2$ negation gates are sufficient to compute NEG^{n-2} by a depth $D+1$ threshold circuit, i.e., $\pi(\nu-2,D)\geq n-1$. From $\pi(\nu-1,D)=n$ and the maximality of π, $\pi(\nu-2,D)\leq n-1$, and it implies $\pi(\nu-2,D)=n-1$.

From the definition of π, $\pi(\nu-1,D)$ can be represented as $\prod_{i=1}^{D}(1+\nu_i)$ such that $\nu_1,\ldots,\nu_D$ are non-negative integers satisfy $\sum_{i=1}^{D}\nu_i=\nu-1$. Then, from Lemma 5.2.2, $\pi(\nu-2,D)=\prod_{i=1}^{D}(1+\nu'_i)$ where $\nu'_j=\nu_j-1$ for some j, and $\nu'_i=\nu_i$ for $i\neq j$. It implies that

$$n-1=\prod_{i=1}^{D}(1+\nu'_i)=\prod_{i=1}^{D}(1+\nu_i)-\frac{1}{(1+\nu_j)}\prod_{i=1}^{D}(1+\nu_i)=n-\frac{1}{(1+\nu_j)}\prod_{i=1}^{D}(1+\nu_i)\,,$$

and thus we have $\prod_{i=1}^{D}(1+\nu_i)=1+\nu_j=n$ and $\nu=n$. It implies that there are

$n = \nu = \sigma(n, D)$ negation gates in C. Note that $\sigma(n, D) = n$ if and only if $D \leq 1$ or $n \leq 2$ (it can be easily verified). Therefore, there is at most one negation output gate. ■

From this lemma, in any depth $D + 1$ (> 2) negation-limited inverter there are at least $n - 1$ monotone gates if $\sigma(n, D) = \sigma(n - 1, D) + 1$, otherwise there are at least n monotone gates. We obtain the following lower bound.

Theorem 6.2.7 *Any depth $D + 1$ (> 2) negation-limited inverter (with $n > 2$) has size at least $\sigma(n - 1, D) + n$.*

Note that the lower bound matches the upper bound shown in Theorem 6.2.5.

Corollary 6.2.8 *The minimum size of depth $D + 1$ (> 2) negation-limited inverters is $\sigma(n - 1, D) + n$.*

6.3 Threshold circuits for Boolean functions

In this section, we consider the size of threshold circuits computing an arbitrary Boolean function.

Lemma 6.3.1 *Let f be an arbitrary Boolean function. Any depth $D+1$ threshold circuit computing f contains at least* $\min\{\, \sigma(d(f), D), \sigma(d(\neg f), D) + 1 \,\}$ *negation gates.*

Proof. Suppose a depth $D+1$ threshold circuit C computing f is given, where C contain ν negation gates. Assume without loss of generality that there is at most one gate, i.e., the *output gate*, in level $D + 1$ of C. Otherwise, by eliminating all gates in level $D + 1$ except the output gate, we can obtain a depth D' ($\leq D + 1$) threshold circuit computing f with smaller size and the number of negation gates in it is not more than ν. Let ν_{D+1} be the number of negation gates in level $D+1$ of C. Then, we have $\nu_{D+1} = 0$ or $\nu_{D+1} = 1$.

Case 1. $\nu_{D+1} = 0$, i.e., the output gate of C is a monotone gate. By the same argument of Theorem 5.2.1, $\nu \geq \sigma(d(f), D)$.

Case 2. $\nu_{D+1} = 0$, i.e., the output gate G of C is a negation gate. By replacing G by an appropriate monotone gate, we can obtain a depth $D + 1$ threshold circuit C'

computing $\neg f$ such that C' contains $\nu - 1$ negation gates and the output gate of C' is a monotone gate. By the same argument of Case 1, we have $\nu - 1 \geq \sigma(d(\neg f), D)$.

Thus, we have

$$\nu \geq \min\{\, \sigma(d(f), D), \sigma(d(\neg f), D) + 1 \,\}.$$

Therefore, there are at least $\min\{\, \sigma(d(f), D), \sigma(d(\neg f), D) + 1 \,\}$ negation gates in C. ■

Note that in Case 1 of the above lemma, there are at least one monotone gate, i.e., the output gate, in C. Thus, we obtain a lower bound on size as follows.

Theorem 6.3.2 *Let f be an arbitrary Boolean function. Any depth $D + 1$ threshold circuit computing f has size at least* $\min\{\, \sigma(d(f), D), \sigma(d(\neg f), D) \,\} + 1$. ■

6.4 Threshold circuits for $PARITY^n$

In this section, we consider the *size* of threshold circuits computing $PARITY^n$. Since $PARITY^n$ is not computable by a depth 1 threshold circuit, we consider only depth $D + 1 \geq 2$ threshold circuits computing $PARITY^n$.

From Theorem 6.3.2 and $\lfloor n/2 \rfloor = d(PARITY^n) \leq d(\neg PARITY^n) = \lceil n/2 \rceil$, we obtain the following lower bound.

Corollary 6.4.1 *Any depth $D + 1$ (≥ 2) threshold circuit computing $PARITY^n$ has size at least $\sigma(\lfloor n/2 \rfloor, D) + 1$.* ■

As an upper bound, we show that a depth $D + 1 \geq 2$ threshold circuit computing $PARITY^n$ can be constructed as follows.

Lemma 6.4.2 *For arbitrary positive integers $M_1, \ldots, M_{D+1}$ satisfying $M_1 \cdots M_{D+1} \geq n + 1$ and $M_{D+1} = 2$, there exists a depth $D + 1$ threshold circuit computing $PARITY^n$ with size $\sum_{i=1}^{D} M_i - D + 1$.*

Proof. From Theorem 5.3.4, we can construct a depth $D+1$ threshold circuit computing $F_2' = (f_0, f_1)$ with size $\sum_{i=1}^{D+1} M_i - D$. Note that $f_0 = PARITY^n$ and f_0 is computed

independently of f_1 in such a threshold circuit, i.e., f_0 and f_1 is computed in parallel. Thus, by eliminating the negation gate computing f_1, we obtain a depth $D+1$ threshold circuit computing $PARITY^n$ with size $\sum_{i=1}^{D+1} M_i - D - 1 = \sum_{i=1}^{D} M_i - D + 1$. ∎

For the smallest j such that

$$\left\lceil \left(\left\lfloor \frac{n}{2} \right\rfloor + 1 \right)^{1/D} \right\rceil^{j} \left\lfloor \left(\left\lfloor \frac{n}{2} \right\rfloor + 1 \right)^{1/D} \right\rfloor^{D+j} \geq \left\lfloor \frac{n}{2} \right\rfloor + 1 = d(PARITY^n) + 1 \geq \frac{n+1}{2}\,,$$

By putting $M_1 = \cdots = M_j = \lceil (\lfloor n/2 \rfloor + 1)^{1/D} \rceil$, $M_{j+1} = \cdots = M_D = \lfloor (\lfloor n/2 \rfloor + 1)^{1/D} \rfloor$, and $M_D = 2$, we have

$$M_1 \cdots M_{D+1} = 2M_1 \cdots M_D \geq 2\left\lfloor \frac{n}{2} \right\rfloor + 2 \geq n+1\,,$$

and

$$\sum_{i=1}^{D} M_i - D = \sigma(\lfloor n/2 \rfloor, D) = \sigma(d(PARITY^n), D)\,.$$

Thus, we obtain the following theorem.

Theorem 6.4.3 *There exists a depth $D+1$ threshold circuit computing $PARITY^n$ with size $\sigma(d(PARITY^n), D) + 1$.*

Note that such a threshold circuit contains the minimum number of negation gates. Furthermore, this upper bound matches the lower bound shown in Corollary 6.4.1.

Corollary 6.4.4 *The minimum size of depth $D+1$ threshold circuits computing $PARITY^n$ is $\sigma(d(PARITY^n), D) + 1$.*

6.4.1 Polylog size threshold circuits for $PARITY^n$

Here we discuss the open problem which posed by Wegener [21].

> **Open problem:** *Determine the minimum depth such that the parity function have circuits of polylogarithmic, i.e., $\log^{O(1)} n$, size.*

Since we have showed the minimum size of depth D threshold circuits computing $PARITY^n$ for any $D > 1$, we can construct a threshold circuit computing $PARITY^n$ with minimum depth for a given size. Thus, the above open problem is *completely solved.*

In the following, we roughly estimate the minimum depth of threshold circuits computing $PARITY^n$ with polylogarithmic, i.e., $\log^{O(1)} n$, size.

Corollary 6.4.5 *Any threshold circuit computing $PARITY^n$ with size $\log^v n+1$ has depth at least $(\log(n+1)-1)/(1+v\log\log n)+1$.*

Proof. Let $D+1$ be the minimum depth of threshold circuits computing $PARITY^n$ with size $\log^v n + 1$. First, note that we can construct a depth $\lceil \log(n+1) \rceil$ threshold circuit computing $PARITY^n$ which has size $\lceil \log(n+1) \rceil$. Thus, we have $D < \lceil \log(n+1) \rceil$. Since circuits constructed in Theorem 6.4.3 has minimum size with respect to depth, we can construct a depth $D+1$ threshold circuit computing $PARITY^n$ which consists of $\log^v n$ negation gates, where $\log^v n = \sigma(\lfloor n/2 \rfloor, D)$. Thus, the lower bound of D can be roughly estimated as follows.

$$
\begin{aligned}
& & \pi(\log^v n, D) &\geq \lfloor n/2 \rfloor + 1 \\
&\Rightarrow & (1+(\log^v n)/D)^D &\geq (n+1)/2 \\
&\Rightarrow & D &\geq \frac{\log(n+1)-1}{\log(1+(\log^v n)/D)} \\
& & &> \frac{\log(n+1)-1}{(\log(D+(\log^v n))-\log D)} \\
& & &> \frac{\log(n+1)-1}{\log(\log n+(\log^v n))} \\
& & &> \frac{\log(n+1)-1}{(1+v\log\log n)}.
\end{aligned}
$$

■

6.5 Conclusion

We show the minimum size of depth D (> 2) threshold circuits, which contains minimum number of negation gates, computing NEG^n and $PARITY^n$. For the case $D = \lceil \log(n+$

$1)\rceil$, we can obtain the depth D threshold circuits computing $PARITY^n$ which constructed by Wegener [21]. For the case $D = \lceil \log(n+1) \rceil + 1$, we can obtain the depth D threshold circuits computing NEG^n constructed by Akers [2].

As an application of negation-limited circuit complexity, we obtain a lower bound on size of threshold circuits computing an arbitrary Boolean function. This is an improvement of the result shown by Wegener [21]. In particular, such a lower bound *matches* the upper bound for $PARITY^n$, i.e., the minimum size of depth D threshold circuit computing $PARITY^n$ is obtained. From this result, an open problem posed by Wegener [21] is *completely solved*.

Although such a lower bound is at most linear of n, it seems that the technique to prove the minimum number of negation gates is useful to prove lower bounds on size for some simple Boolean functions.

Chapter 7

Conclusions

In this thesis, we have shown some results on the complexity of negation-limited circuits. First for the negation-limited circuits over basis $\{ \wedge, \vee, \neg \}$, we have shown lower bounds on the size and the depth. In particular, we have obtained a $5.33n$ lower bound on the size of negation-limited circuits computing parity functions. Furthermore, we have shown that there exist negation-limited circuits computing some symmetric functions whose depth match our lower bound.

Next, we deal with the complexity of negation-limited inverters. We have shown an upper bound on the depth of negation-limited inverters. Our upper bound improve the previous result by a factor of 3, and it possibly matches the lower bound shown by Tanaka and Nishino [18]. By using the lower bound on the size of negation-limited circuits computing parity functions, we have also obtained a 7.33 lower bound on the size of negation-limited inverters. Moreover, as main results, we have shown an $\Omega(n \log n)$ lower bound on the size of negation-limited inverter under a natural assumption. That is, if

$$D^0(T^n_{\lceil n/2 \rceil}) = D^0(T^n_1, \ldots, T^n_n),$$

any minimum depth negation-limited inverter has size at least $2n \log n + 3n$.

We also studied the negation-limited threshold circuits. First, we consider the minimum number of negation gates in threshold circuits. We have shown that the result of Santha and Wilson [14] can be slightly improved. That is, we have shown a lower bound on the minimum number of negation gates in a threshold circuit computing an arbitrary

Boolean function. The Markov's lower bound can obtained as a special case of our lower bound. Furthermore, we have shown an upper bound on the minimum number of negation gates in threshold circuits computing some Boolean functions which matches our lower bound. It implies that our lower bound is *tight*.

On the other hand, we have shown that the lower bound on the minimum number of negation gates in threshold circuits computing any single-output Boolean functions and inverters can be improved. We also consider the size of the negation-limited threshold circuits. We have shown the minimum size of threshold circuits computing inverters and parity functions. Finally, as an application of negation-limited circuit complexity, we have shown a lower bound on the size of general threshold circuits computing an arbitrary Boolean function, by using the lower bound on the minimum number of negation gates. In particular, such a lower bound matches our upper bound on the size of negation-limited threshold circuits computing parity functions. That is, the minimum size of general threshold circuits computing parity functions is obtained.

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