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A Study of Dynamic Code Optimization Using Hardware Analysis System

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Abstract

In this study, I propose a dynamic optimization system. The system is used to generate an optimized program by modifying original native binary code at run-time. The system consists of two components; The First is the hardware that enables the system user to define trapping conditions for new interrupts. The second is the optimizer routine, which is implemented as a trap hander(operating system) invoked from the hardware. The hardware can also be used for other purposes. For example, the hardware can be used for program debugging support. In addition, a variety of optimization algorithms can be implemented in the system, since the optimizer is implemented as software. In this thesis, I discuss how to implement the system using Alpha CPU as an example.

The system has a characteristic different from conventional compiler optimization; The system can exploit run-time information inside a CPU such as histories of execution. In this thesis, data prefetch optimization is proposed and evaluated as an example of dynamic optimization. We evaluated the optimization using 21 SPEC CPU benchmarks. Results showed that 16 benchmarks got better or at the least same performance compared to recent hardware data prefetch techniques. On the other hand, the system can be implemented with smaller hardware than the recent hardware data prefetch techniques. The hardware data prefetch techniques require from 4 times to 3587 times lager memory area.

In addition, this thesis also discusses the details of implementing program debugging support using the trap hardware. Also software trace optimization is described as an example of other optimization algorithms.

Key Words: **dynamic optimization system, data prefetch, hardware reduction**