Though ordinary process pair techniques required one of more chips, our technique can be realized on one multi-core chip; this could reduce the development cost

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Recently, software is embedded in everywhere, and reliability of embedded software is becoming increasingly important. However, techniques to improve reliability are high-cost generally, and it is difficult to apply them to consumer products whose development-cost limitation is severe. Therefore, for consumer products, cost-effective techniques to improve reliability are required.

However, as mentioned above, these techniques are generally expensive to apply to consumer products. Meanwhile, multi-core chips for embedded device are gradually being used and expected to be used for sophisticated and high-performance embedded systems. In future, high-performance embedded device development that utilized this chip technology are expected.

Purpose of the study is to propose a techniques that improve reliability that can be applicable to consumer systems at acceptable cost and effort. Concretely speaking, we propose a technique that realize "process pair on multi-core chips". We also propose a software framework that support the development of applications based on our technique.

Firstly, we propose a software architecture for realizing "process pair on multi core chips". Though ordinary process pair techniques required one of more chips, our technique can be realized on one multi-core chip;

・this could reduce the development cost.
・to downsize are possible.

In examining the architecture, we consider the following points.

- It is realized on one multi-core chips.
- It could be used for various applications and error types.
- Minimize the application program changes to adopt our technique.

In the development of the consumer product, the limitation of the development period is particularly severe too and to reduce workload is needed for developers. Therefore, we propose a software framework that supports ... it support to apply ‘ process-pair for multi-core chip ’ to application. Purposes of the framework are as follows.

- It supports develop new applications on our method.
- It supports adopt our method to existing applications.
- It will be the basis of realization of "recovery-block" on multi-core chips.

In addition, we have developed a software script that support the development of applications on our framework.

We have evaluate our method and framework.

Evaluation of proposed method:

- Demonstrate functionality by a sample program.
- Measure the performance of switching cores, and shows it is reasonable for consumer products.

Evaluation of proposed framework:

- Measure the size of framework and shows it is acceptable.
- Demonstrate that we can migrate an existing application on single-chip to multi-core chip using our framework.

We believe our proposal could be a support to improve reliability of the consumer products.