Advantage of Plasma-Less Deposition; Cat-CVD Fabrication of a-Si TFT with Current Drivability Equivalent to Poly-Si TFT

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This is to study on the advantage of plasma-less deposition in catalytic chemical vapour deposition (Cat-CVD), often called hot-wire CVD. The effects of plasma damage are particularly studied by the performance of amorphous-silicon thin film transistors (a-Si TFTs), since it is strongly affected by the property of an interface between a gate insulating film and an a-Si film. It is found that the plasma damage at the interface affects on off-current of TFT, and that the off-current of Cat-CVD a-Si TFT is much lower than that of a-Si TFT in which all films are prepared by the conventional plasma-enhanced CVD (PECVD). The off-current of Cat-CVD a-Si TFTs is likely to increase and approach to the same level as the off-current of PECVD a-Si TFT, when Cat-CVD a-Si is exposed to weak plasma. In addition, since the off-current is so low, when the ratio of the channel width (W) to the channel length (L) is adjusted, the on-current can be increased up to the same level as the on-current of poly-crystalline silicon (poly-Si) TFT with keeping the off-current on the same level as that of poly-Si one. That is, it is concluded that a-Si TFT with current drivability equivalent to poly-Si TFT can be produced by using plasma-less Cat-CVD method for preparing films used in TFTs.

1 Introduction Among various deposition techniques, catalytic chemical vapor deposition (Cat-CVD) has unique advantages such as simplicity of deposition apparatus. Device-quality amorphous silicon (a-Si) films are obtained with deposition rates as high as 2 nm/s and with high efficiency of gas use [1,2]. The method has also an important advantage as a plasma-less deposition technique. However, this advantage has been forgotten in fabrication of a-Si devices, although the advantage works successfully for the preparation of Si nitride (SiN_x) coating films on compound semiconductor devices and other devices using feeble materials [3,4].

In fabrication of thin-film devices such as a-Si solar cells and thin-film transistors (TFTs), various films are stacked, and the lower films always suffer from damages during the deposition of the upper films. Here, we particularly investigated the effect of plasma damage in plasma-enhanced CVD (PECVD) onto lower films, and compared it with Cat-CVD. We studied the characteristics of TFT to know the effect of the upper film deposition, since the stability of the TFT characteristics is sensitive for fabrication process. Bottom-gate a-Si TFTs are fabricated by using Cat-CVD SiN_x, n^+-microcrystalline- (μc-) Si or n^+-a-Si films, and the results are compared with PECVD a-Si TFTs. The effects of a-Si deposition on SiN_x or Si dioxide (SiO_2) gate insulators are also investigated by measuring the variation of the TFT characteristics under DC bias stress and current stress. It is found that the on/off current ratio in the transfer characteristics of Cat-CVD a-Si TFTs can be much larger than that of PECVD a-Si TFTs, and reaches to 10^9. The value is likely to degrade easily after Cat-CVD a-Si TFTs are exposed to weak plasma. The large on/off current ratio appears to come from the deposition without plasma damage in Cat-CVD. It is also confirmed that a-Si TFT with current drivability equivalent to that of poly-Si TFTs can be fabricated by Cat-CVD, by adjusting W/L ratio of the TFTs.

2 Fundamentals for Experiment The cross-sectional view of both PECVD and Cat-CVD a-Si TFTs are shown schematically in Fig. 1. Typical fabrication process of the a-Si TFTs is described as follows;

1) Aluminum (Al) and molybdenum (Mo) stacked films 200 nm thick in total or a chromium (Cr) film were formed by sputtering on glass substrates.

2) They were patterned by a photolithography to form the gate electrodes and also gate lines.

3) 400 nm-thick SiN_x gate insulator and a 200 nm-thick a-Si active layer were continuously deposited at 320 °C. Here, PECVD a-Si TFTs were fabricated at a company, which is one of the world top-class suppliers of liquid crystal displays (LCDs). The PECVD a-Si TFTs have commercially sufficient performance and stability for the driving of active-matrix LCDs.

4) n^+-μc-Si or n^+-a-Si films were deposited on such a-Si films.

5) TFT areas were isolated by an etching process, and source and drain electrodes were formed by the back etching of channel positions.

Cat-CVD a-Si TFTs were fabricated on the same glass substrates as those used for PECVD a-Si TFTs. Defect density of a-Si and SiN_x films strongly affects the electric properties and stability of a-Si TFTs. Thus, we carefully optimized their deposition conditions. SiN_x films with the defect density of 1.3×10^{17} /cm^3 and a-Si films with that less than 10^{16} /cm^3 were used for Cat-CVD a-Si TFTs in most of cases. The detailed deposition conditions are summarized in Table I.

Apart from the deposition of SiN_x and a-Si films, other fabrication processes were completely same as those of PECVD a-Si TFTs, in order to compare the performance of Cat-CVD TFTs with PECVD ones. However, in the present paper, just to know the effect of materials of gate insulators in the study on the stability of TFTs, PECVD SiN_x and SiO_2 films were used as gate insulators. Other results shown here are all obtained by the TFT fabricated with the processes described here.

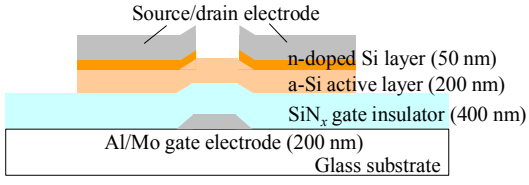

Figure 1 Schematic view of PECVD and Cat-CVD a-Si TFTs.

Table 1 Deposition conditions of Cat-CVD films.

		SiN_x	a-Si	n^+-μc-Si
SiH_4 gas flow rate	(sccm)	6	50	20
NH_3 gas flow rate	(sccm)	300	-----	-----
H_2 gas flow rate	(sccm)	-----	10	200
PH_3 (2% : diluted with He) flow rate	(sccm)	-----	-----	10
Catalyzer temperature (T_{cat})	(°C)	1750	1750	1800
Substrate temperature (T_{sub})	(°C)	330	330	330
Gas pressure (Pa)	(Pa)	15	1.1	1
Distance between catalyzer and substrate (D_{cs})	(cm)	14	12	12

3 Performance of Cat-CVD and PECVD a-Si TFTs Figure 2 demonstrates the transfer characteristics under a drain voltage (V_d) of 10 V in saturation region for both PECVD and Cat-CVD a-Si TFTs with L=4 μm and W= 23 μm. The field effect mobility μ is about 0.6 cm^2/Vs and the on/off current ratio is 10^7 for a PECVD a-Si TFT and 10^9 for a Cat-CVD a-Si TFT. In the figure, it should be noticed that the off-current of Cat-CVD a-Si TFTs is 10^{-15} A, although that of PECVD is 10^{-13} A. The off-current of the Cat-CVD a-Si TFTs is 2 orders of magnitude lower than that of the PECVD ones.

We do not know the exact reason why the off-current of Cat-CVD TFTs becomes lower than that of PECVD ones. One possibility is the influence of the plasma damage on PECVD TFTs. A clear example is demonstrated in Fig. 3. In the figure, The plasma was formed in oxygen gas (O_2) ambient. The plasma itself was quite weak, and the electric power supplied for generation of plasma was just over the value from which plasma generation started. It is clearly observed that a-Si is damaged by this weak plasma and that a ESR signal due to Si dangling bonds come out.

Such plasma damage also degrades the characteristics of a-Si TFTs. Figure 4 shows the transfer characteristics of

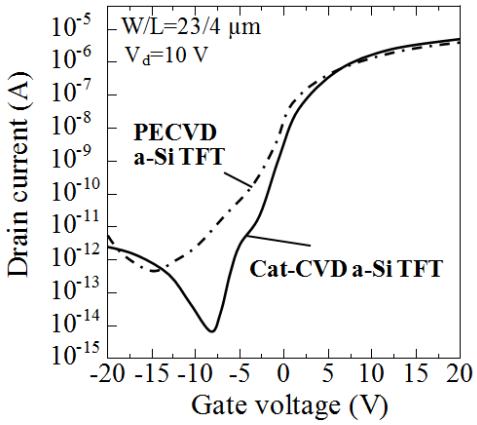

Figure 2 Transfer characteristics of PECVD and Cat-CVD TFTs.

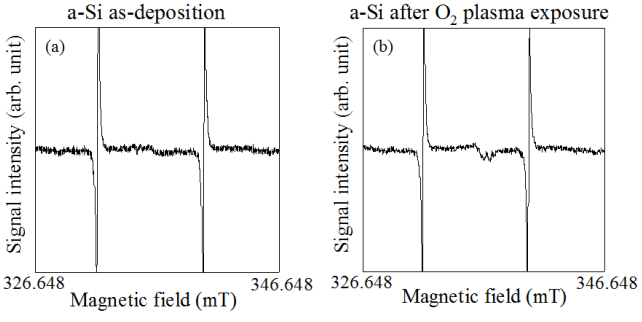

Figure 3 ESR data of a-Si films before (a) and after (b) plasma exposure.

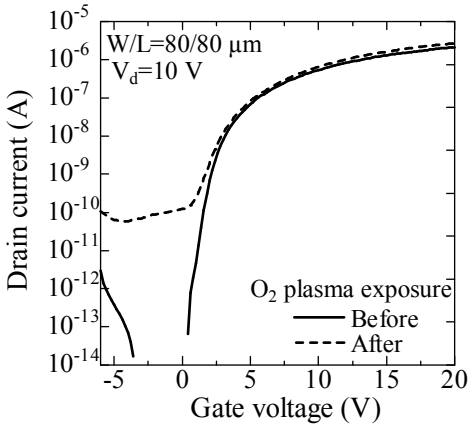

Figure 4 Transfer characteristics of Cat-CVD a-Si TFT before and after exposure to O_2 plasma.

Cat-CVD a-Si TFTs before and after exposure to the weak plasma in O_2 ambient. TFTs shown schematically in Fig. 1 were simply installed in plasma chamber. Thus, a-Si layer at the position of a back channel might be damaged, and the electron transport through defect states might be added in the off-current. In the conventional fabrication process in PECVD a-Si TFTs, all area of TFTs is covered with a SiN_x passivation film. This process may cause the increase of the off-current, although we have not checked yet how the off-current behaves when only the final passivation films in PECVD a-Si TFTs are prepared by Cat-CVD.

4 Instability of a-Si TFTs When a-Si films are deposited on gate insulator, the plasma may make damage on gate insulating films. When the gate insulator is damaged, the trap states are formed there, and they may cause the instability such as threshold voltage (V_{th}) shift in a-Si TFTs due to charge trapping.

Here, V_{th} shift after DC-gate bias stress and current stress are observed for 3 types of bottom gate a-Si TFTs. For only this experiment, TFTs were specially prepared apart from the fabrication conditions described in chapters 2 and 3. Type a) has a structure of Cat-CVD a-Si/PECVD SiO_2 gate insulator/gate-metal/glass, type b) has Cat-CVD a-Si/PECVD SiN_x gate insulator/gate-metal/glass, and type c) has PECVD a-Si/PECVD SiN_x gate insulator/gate-metal/glass. Two types of stresses were also applied on such 3 types of a-Si TFTs. One was applying gate voltage (V_g) of 30 V but no drain voltage (V_d), and second was applying both V_g=35 V and V_d=20 V. The first one is called DC bias stress and the second one is current stress.

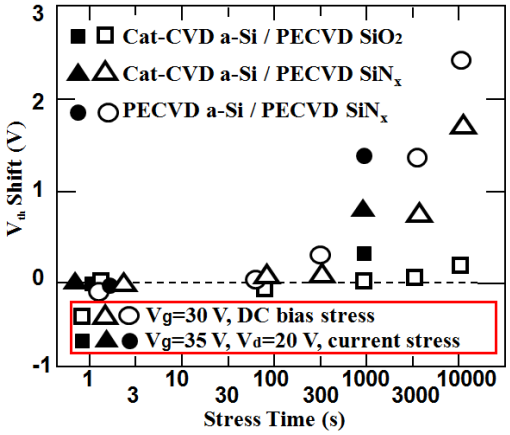

Figure 5 V_{th} shift of a-Si TFTs as a function of stress time.

Figure 5 shows V_{th} shift for 3 types of a-Si TFTs as a function of stress time. It is firstly found that V_{th} shift is negligibly small when a PECVD SiO_2 film is used as a gate insulator a below Cat-CVD a-Si channel layer, even when the DC stress was applied for 10^4 s and the current stress for 10^3 s. When a Cat-CVD a-Si layer is deposited on PECVD SiN_x gate insulator, slight shift of V_{th} can be detected. However, the V_{th} shift became more apparent, when a PECVD a-Si layer was deposited on a PECVD SiN_x gate insulating layer.

The difference between types b) and c) TFTs can be understandable, because plasma damage is introduced inside the PECVD SiN_x gate insulating layer during a-Si deposition. Newly generated trap states in the gate insulator will cause the shift of V_{th}. PECVD SiN_x films probably have certain trap states before a-Si films are deposited and the effect of plasma-less deposition of Cat-CVD may be masked. Even so, the V_{th} shift of type b) TFT appears smaller than that of type c) TFTs.

The reason why TFT with SiO_2 gate insulator is stable is not clear at the moment. We have not measured the initial defect density of PECVD SiO_2 and SiN_x films. Thus, we cannot say exact mechanism for the difference of stability. When a-Si films are deposited, the layer below it may suffer from not only plasma damage but also hydrogen attack. It is known that high density hydrogen can etch a substrate. If PECVD SiN_x films are not perfect, it would be suffer from both plasma damage and hydrogen etching to make rough interface. However, perfect SiO_2 is very tough for such hydrogen attack. This may be one possible reason to explain the results of Fig. 5. Anyway, it is suggested that Cat-CVD a-Si TFTs can be very stable if proper gate insulator is provided.

5. High Current Drivability of Cat-CVD a-Si TFTs As mentioned above, Cat-CVD a-Si TFT can be used as a new type a-Si TFTs with extremely high stability. Thus, if the high current drivability can be added to this, a-Si TFT equivalent to poly-Si TFTs can be produced by using Cat-CVD technology. The remarkably low off-current in all Cat-CVD a-Si TFTs enables to realize TFTs with high on-current, equivalent to poly-Si TFTs by simply increasing the W/L ratio keeping the low off-current still low enough.

Figure 6 shows a-Si TFTs with comb-like source and drain electrodes, by which large W/L can be realized without enlarging TFT area. Figure 7 shows the transfer characteristics of the Cat-CVD a-Si TFTs with comb-like elec-

trodes having W of 25, 1000 and 5000 µm and L of 5 µm for V_d=8 V. In the figure, typical transfer characteristics of a lightly-doped-drain (LDD) poly-Si TFT with the mobility µ of 210 cm^2/Vs are also demonstrated for comparison. Even if the W of the Cat-CVD a-Si TFTs increases up to 1000 or 5000 µm, the off-current is still smaller than that of the poly-Si TFTs. On the other hand, it is shown that the on-current of Cat-CVD a-Si TFTs is equivalent to the poly-Si TFTs.

The time used for electron transport between source and drain electrodes is expressed by $(4/3)L^2/(\mu V_d)$ when the space charge has to be taken into account for high resistivity materials such as a-Si. The transit time through the channel is about 0.1 µs for L=5 µm and µ is only 0.3 cm^2/Vs. The value is enough for the pixel control of organic electro-luminescence displays or other circuit controllers. This appears suggestive for feasibility of Cat-CVD a-Si TFTs, which is fabricated with plasma-less deposition.

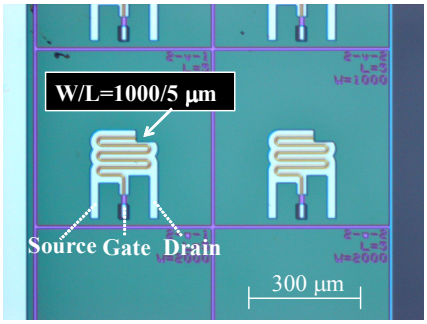

Figure 6 a-Si TFTs with comb-like source and drain electrodes.

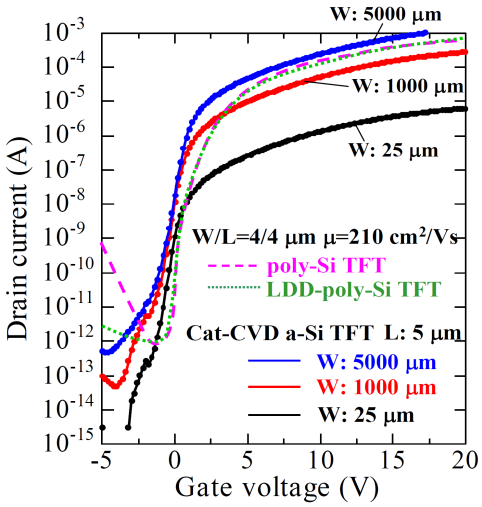

Figure 7 Transfer characteristics of the Cat-CVD a-Si TFTs with comb-like electrodes.

6. Conclusion From the above results, the follows are concluded;

1) Cat-CVD a-Si TFTs with current drivability equivalent to that of poly-Si TFTs can be prepared by increasing W/L, since the off-current of Cat-CVD a-Si TFTs is almost 2 orders of magnitude smaller than that of PECVD a-Si TFTs.

2) Low off-current appeared in Cat-CVD a-Si TFTs is probably due to the low damage process of Cat-CVD.

3) According to preliminary experiment using PECVD SiO_2 and SiN_x films as gate insulators, it is found that best stability appears seen when a Cat-CVD a-Si active channel layer is deposited on SiO_2 gate insulator.

4) If proper gate insulator is provided to Cat-CVD a-Si TFTs, highly stable a-Si TFT will be realized, which has excellent current drivability just like poly-Si TFTs.

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