Thin Solid Films, **518**, 534-536 (2009)

An organic nonvolatile memory using space charge polarization of a gate dielectric

Kodai Konno, Heisuke Sakai, Toshinori Matsushima, Hideyuki Murata*

School of Materials Science, Japan Advanced Institute of Science and Technology,

1-1 Asahidai, Nomi, Ishikawa 923-1292, Japan

Abstract

We realize a nonvolatile and rewritable memory effect in an organic field-effect transistor (OFET) structure using polymethylmethacryrate (PMMA) dispersed with 10-methyl-9-phenylacridinium perchlorate ($MPA^+ClO_4^-$) as a gate dielectric. Applying a voltage between a top source-drain electrode and a bottom gate electrode induces electrophoresis of two ions of MPA^+ and ClO_4^- toward the corresponding electrodes in the memory devices. The drain currents of the memory devices markedly increase from 10^{-9} A to 10^{-2} A under no gate voltage condition due to the strong space charge polarization effect. Our memory devices have excellent electrical bistability and retention characteristics, i.e. the memory on/off ratio reached 10^7 and the drain current maintained 40% of the initial value after 10^4 s.

Thin Solid Films, **518**, 534-536 (2009)

Keywords: Organic nonvolatile memory, organic field-effect transistor (OFET), gate dielectric, space charge polarization, polymethylmethacryrate (PMMA), 10-methyl-9-phenylacridinium perchlorate ($MPA^+ClO_4^-$)

* Corresponding author. Tel.: +81 761 51 1531; fax: +81 761 51 1149.

E-mail address: murata-h@jaist.ac.jp (H. Murata)

1. Introduction

Nonvolatile memory devices are indispensable elements for manufacturing electronic circuits. In particular, organic nonvolatile memory devices comprising small organic molecules and polymers have attracted considerable attention due to their high potentials for use in low-cost, large-area, and flexible applications [1-10]. The organic memory devices have frequently been fabricated based upon an organic field-effect transistor (OFET) structure [3-10]. Excellent bistable characteristics were realized when using a ferroelectric material of poly(vinylidene fluoride/trifluoroethylene) as a gate dielectric [7-10]. Thus, the key technique commonly used in the OFET-type memory devices reported to date was controling the polarization in a gate dielectric layer to induce accumulation of carriers in a channel region. However, their small memory on/off ratios and memory retention times are still problematic and need to be further improved for the practical applications. Additionally, the ferroelectric materials used as gate dielectrics of the OFET-type memories are limited. Thus, the development of new gate dielectrics for the OFET-type memories is of great importance.

In this study, we propose space charge polarization of a gate dielectric layer as a versatile method to fabricate high-performance OFET-type memory devices. To obtain the space charge

polarization effect, we used polymethylmethacryrate (PMMA) dispersed with 10-methyl-9-phenylacridinium perchlorate ($MPA^+ClO_4^-$) as a gate dielectric. By applying a voltage between a top source-drain electrode and a bottom gate electrode, MPA^+ and ClO_4^- ions migrate in opposite directions to form space charge polarization in the gate dielectric. Recently, we reported that threshold voltages of OFETs can be shifted by using the space charge polarization of the similar PMMA:$MPA^+ClO_4^-$ system [11]. Due to the strong space charge polarization effect, we demonstrated that a large number of holes were accumulated in a channel region without a gate bias and drain currents of the OFETs were increased. Using the above-mentioned technique, we demonstrated high-performance nonvolatile and rewritable memory devices with a high on/off ratio and a high retention time.

2. Experimental

The schematic structure of our OFET-type memory devices is shown in the inset of Fig. 1(a). A glass substrate coated with a 150 nm indium tin oxide (ITO) layer was used as a gate electrode. The substrates were cleaned using ultrasonication in acetone, detergent, pure water, and isopropanol. After the ultrasonication, the substrates were placed in an UV-ozone cleaner for 30 min. PMMA and $MPA^+ClO_4^-$ were dissolved in acetonitrile to prepare a 5 wt% solution where

the molar ratio of a monomer unit of PMMA to MPA^+ClO_4 was fixed at 50/1. A PMMA composite gate dielectric layer was spin-coated from the solution at 1500 rpm for 90 s. The thickness of the gate dielectric was measured to be 400 nm using DEKTAK surface profilometry. A 30 nm pentacene layer with a high hole mobility [12,13] was vacuum-evaporated on the gate dielectric layer at a rate of 0.02-0.03 nm/s under a base pressure of $< 5 \times 10^{-4}$ Pa. To complete the devices, a 50 nm Au layer was vacuum-evaporated on top of the pentacene layer at a rate of 0.04 nm/s through a shadow mask with openings to form source and drain electrodes with a channel length of 75 μm and a channel width of 24.5 mm. The devices were transferred to a dry nitrogen-filled glove box. The output and transfer characteristics of the devices were measured with a Keithley 4200 semiconductor characterization system in the glove box at room temperature (27ºC).

To evaluate the memory characteristics of the devices, a voltage (V_{TB}) was applied between the top Au source-drain electrode and the bottom ITO gate electrode for certain duration (t_{TB}) to induce the space charge polarization (the "write" cycle). After the V_{TB} was stopped, the drain currents (I_D) were measured at a source-drain voltage (V_{SD}) of -15 V and a gate voltage (V_G) of 0V (the "read" cycle). For the "erase" cycle, the reversed V_{TG} was applied to the devices for the

similar t_{TB}. The memory characteristics of the devices were measured using a Keithley 2400 source meter in the glove box.

3. Results and discussion

3. 1. FET characteristics

Our doped FETs had the typical *p*-type output characteristics, depicted as I_D vs. V_{SD} at various gate voltages V_G (Fig. 1(a)), where V_{SD} was swept at a speed of 0.1 V/s at a certain V_G. The results showed that I_D increases linearly with V_{SD}, and, after the V_{SD} reaches a certain voltage, the I_D becomes saturated as the accumulation of holes in the pentacene layer is pinched off.

Figure 1(b) shows the transfer characteristics of the FET devices, depicted as I_D vs. V_G and $I_D^{0.5}$ vs. V_G at a constant V_{SD} of -30 V. The transfer characteristics were measured by sweeping V_G from 30 V to -30 V at a speed of 0.1 V/s (the forward bias direction), followed by sweeping V_G from -30 V to 30 V at the same speed (the reverse bias direction). The hole mobility (μ) and the threshold voltage (V_{TH}) of the devices can be calculated from a saturation regime using the conventional metal-oxide semiconductor equation, [14] $I_{D,SAT} = \{\mu WC(V_G-V_{TH})^2\}/(2L)$, where $I_{D,SAT}$ is the saturated drain current, W is the channel width (24.5 cm), L is the channel length (75

μm), and C is the capacitance per unit area of the dielectric (8.63 nF/cm^2 measured from pure PMMA). Fitting the $I_D^{0.5}$-V_G curves shown in Fig. 1(b) with the equation gave a μ of 0.25 cm^2/V s and a V_{TH} of 15.4 V in the forward bias direction and a μ of 0.19 cm^2/V s and a V_{TH} of 11.6 V in the reverse bias direction. The current on (V_G = -30 V)/off (V_G = 0 V) ratios of the FETs were 10^4 in the forward bias direction and 10^2 in the reverse bias direction.

While the μ was almost unchanged, we observed the threshold voltage shift and the change of the on/off ratios (see Fig. 1(b)). Moreover, we found that the transfer characteristics are changed from a normally-off state to a normally-on state, depending upon the bias directions. The ratio of the I_D obtained in the different bias directions at a V_G of 0 V was 120. These results indicate that the strong space charge polarization of the gate dielectric occurs by simply applying the V_G and induces the accumulation of holes in the channel region at a V_G of 0V [5-10]. The advantage of our memory devices is that the "read" cycle can be performed without applying V_G.

3. 2. Memory characteristics

The room-temperature I_D vs. t_{TB} characteristics at various V_{TB} are shown in Fig. 2(a). The I_D gradually increased with increasing the t_{TB} and the V_{TB} due to the gradual electrophoresis of

MPA^+ and ClO_4^- toward the corresponding electrodes. When using the t_{TB} of 600 s and the V_{TB} of -60 V, we obtained a very high I_D of 3×10^{-2} A and the memory on/off ratio achieved a very high value of 10^7. This ratio is two orders of magnitude higher than those of OFET-type memory devices previously reported [3-10].

We also checked whether the I_D returned to the initial values by applying the reversed V_{TB} to the devices for the similar t_{TB} (the "erase" cycle). We confirmed that the write-read-erase cycles were repeatable without the change of maximum I_D and minimum I_D, meaning that the memory devices are rewritable. Based on these results, we conclude that the space charge polarization is advantageous to the fabrication of nonvolatile and rewritable organic memory devices.

We investigated the retention characteristics of the memory devices. After the V_{TB} of -30 V was applied to the devices for various t_{TB} (0, 5, 10, 20, 30, and 60 min), the changes of the I_D were measured as a function of retention time (see Fig. 2(b)). In every device, the I_D decreased to 40% of the initial values after 10^4 s. The retention time of the memory devices is comparable to those of previously reported devices [3-10].

Since migration rates of ions depend on sample temperature [15-16], we investigated how the device temperature affects the writing times of our memory devices. The device temperature was changed in a range from 27ºC to 80ºC to measure the temperature dependence of the writing time. The glass transition temperature of PMMA used in this study is 96ºC. Figures 3(a) and 3(b) show the I_D vs. t_{TB} characteristics at various device temperature and the writing time vs. reciprocal device temperature characteristics, respectively. We defined the writing time shown in Fig. 3(b) as the time when the memory on/off ratio of 10^5 was obtained in Fig. 3(a). The maximum I_D reached at a same value of $\approx 10^{-1}$ A at the device temperatures higher than 40ºC. However, we found that the writing times decrease with increasing the device temperature (Fig. 3(b)). The writing time (7 s) at 80ºC was about two orders of magnitude shorter than that (1750 s) at 27ºC. Moreover, the experimental curve shown in Fig. 3(b) can be well explained using a Williams-Landel-Ferry model [15,16] rather than an Arrhenius model, indicating that the writing times of the memory devices are limited by an electrophoresis process of MPA^+ and ClO_4^- in the doped gate dielectric.

The memory devices are expected to possess very good write-read-erase cycle

characteristics at the elevated temperature due to the decrease in the writing time as discussed previously. Thus, the repetition test of the write-read-erase cycles was performed at 80ºC for the memory devices. When the V_G was changed as shown in Fig. 4(a), the memory devices exhibited excellent response of the I_D to the applied V_G (Fig. 4(b)). After the V_G was stopped, the I_D dropped about 80% of the initial currents. However, it should be emphasized that the memory on/off ratio of the devices still maintained about 10^3.

4. Conclusion

We demonstrated a nonvolatile and rewritable memory effect in an organic field-effect transistor (OFET) structure using PMMA dispersed with $MPA^+ClO_4^-$ as a gate dielectric. Our memory devices had excellent electrical bistability and retention characteristics, i.e. the memory on/off ratio achieved 10^7 and the drain current maintained 40% of the initial value after 10^4 s. From results of temperature dependence on memory characteristics, we found that writing times of the memory devices are limited by an electrophoresis process of MPA^+ and ClO_4 in the PMMA gate dielectric layer. Thus, we believe that the OFET with an ion-dispersed polymer dielectric will be a promising candidate as an organic memory device.

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Figure captions

Fig. 1. (a) Output characteristics, I_D vs. V_{SD} at various gate voltage V_G, and (b) transfer characteristics, I_D vs. V_G and $I_D^{0.5}$ vs. V_G at constant V_{SD} of -30 V, of FET devices. Inset in (a) shows schematic FET structure.

Fig. 2. (a) Room-temperature I_D vs. t_{TB} characteristics at various V_{TB} and (b) I_D-retention time characteristics as function of t_{TB} of memory devices. V_{SD} was fixed at -15 V.

Fig. 3. (a) I_D vs. t_{TB} characteristics as function of device temperature and (b) writing time-reciprocal device temperature characteristics of memory devices. V_{SD} and V_{TB} were fixed at -15 V and -30 V, respectively. Device temperature was changed ranging from 27ºC to 80ºC.

Fig. 4. Repetition test of write-read-erase cycles of memory devices at 80ºC. When V_G was changed in manner shown in (a), I_D was measured at V_{SD} of -15 V (b).

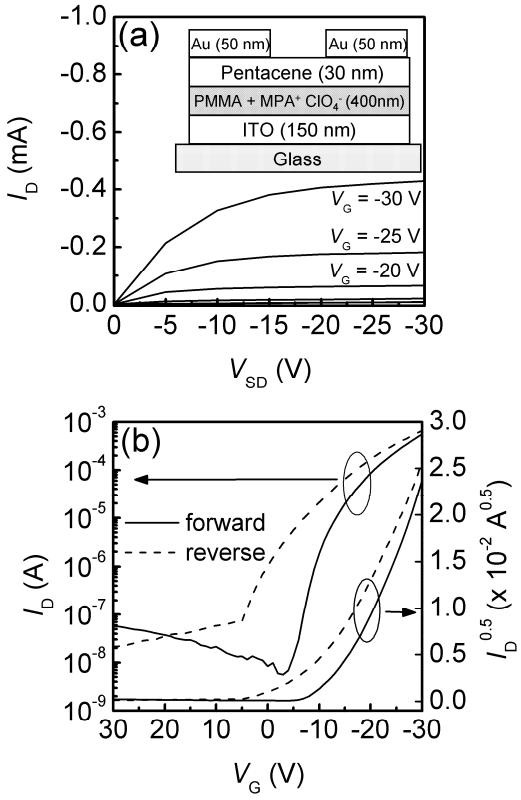

Fig. 1.

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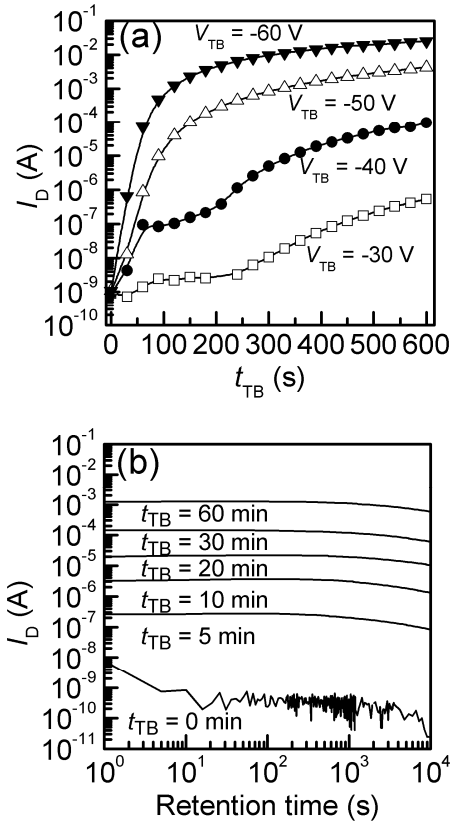

Fig. 2.

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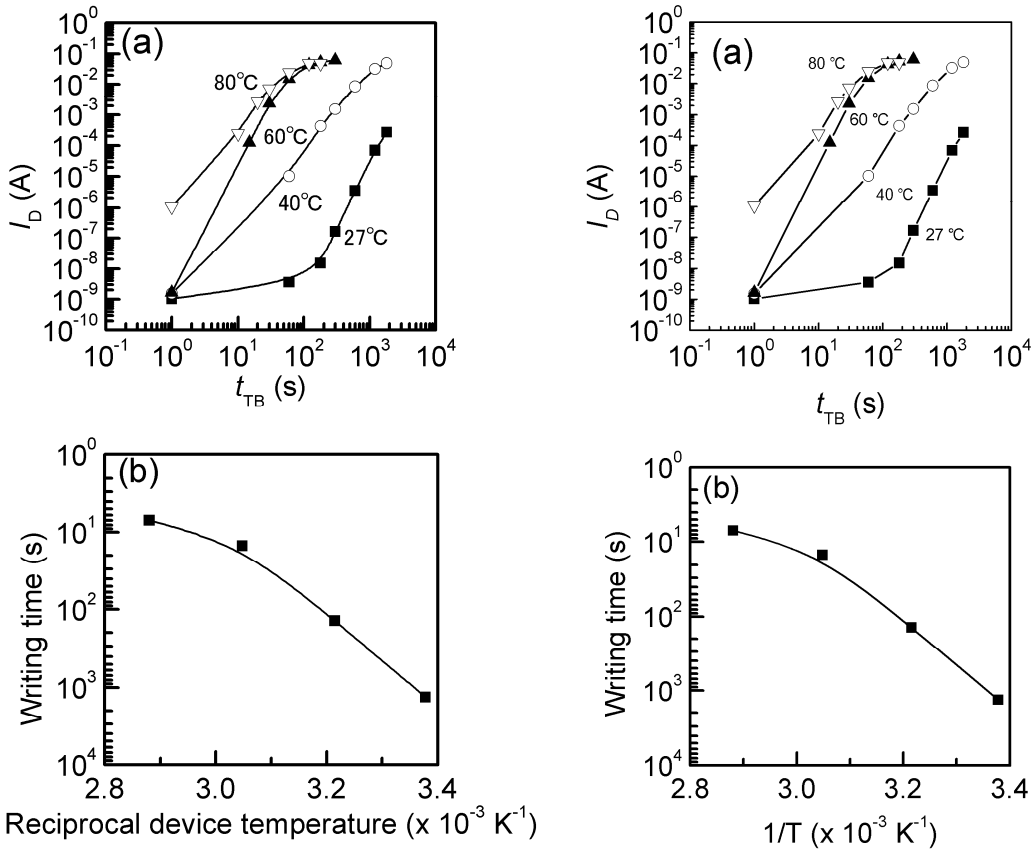

Fig. 3.

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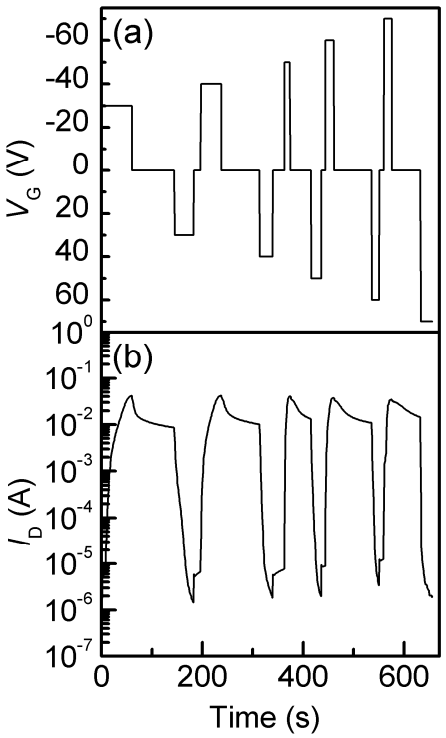

Fig. 4.

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