Assignment-Centric Approach to Data-Path Synthesis for Application Specific VLSIs

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January 9, 2003

Abstract

Most of the conventional high-level synthesis aim mainly to minimize the number of control steps and the number of functional units, and they first decide the schedule and the number of functional units by resource constrained scheduling or time constrained scheduling, which are followed by resource assignment. However, the connectivity between modules is also an important metric for VLSIs for its connection with wire complexity, transmission delay, power consumption, testability, etc. In order to handle interconnection-related metric more accurately, simultaneous scheduling and assignment approach and assignment-driven approach are proposed. In those approaches, we often encounter a scheduling problem with specified resource assignment, which becomes one of the most importance core tasks in high-level synthesis. We study a loop pipeline scheduling problem under given resource assignment.

In this thesis, (1) we treat both assignment of operations to functional units and assignment of data to registers, (2) we introduce disjunctive arcs with variable weights to scheduling graph for representing constraints induced by assignment specification, (3) we formulate the range of available value for each un-fixed variable, (4) we construct a branch-and-bound method incorporated with successive refinement of those ranges, (5) we present a heuristic method to find a schedule having the minimum iteration period based on the reduction of those ranges using sensitivity to iteration period, (6) we extend our variable disjunctive arc approach to assignment constrained scheduling for dependence graph with conditional branches, and (7) we derive a branch-and-bound method and a heuristic method incorporated with successive refinement of parameter space.

Finally, we have developed a high-level synthesis system based on a new strategy for exploring solution space, and demonstrated its high ability in synthesizing cost optimal data-paths, especially in reducing connection-relevant hardware resource. Most important feature of our assignment-centric approach is its ability to control connectivity between modules, and a higher level of design optimization considering transmission delay and transmission power can be achieved by incorporating floorplan into our system.

Key Words: VLSI design, data-path synthesis, resource assignment, pipeline schedule, disjunctive arc, longest path