# Research for fabrication and characterization of solution-processed ferroelectric-gate thin-film transistors and their characterization

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## 1. Introduction

Today, the current nonvolatile memory mainstream is based on the floating-gate flash technology, which has more than 90% market share. Although the flash memory has been able to follow the evolution of the semiconductor roadmap for next 10 years and it is expected to scale with the same trend for the next technology nodes, because of the performance limitations, it cannot replace the SRAM memories.

Even though RAM devices have fast read/write time and unlimited number of cycles, they require power to maintain memory state. Also, ROM devices are nonvolatile but it is slow to write and limited number of write/read cycles ($10^6$). Therefore, an ideal memory technology should combine high speed read and write, high endurance, high packing density and low operation voltage.

A ferroelectric-gate field-effect transistor has attracted much attention as a nonvolatile memory element with low power consumption, high speed, and high endurance owing to the ferroelectric nature and such a transistor is applicable for various applications including wireless IC cards and tools for mobile communications.[1,2] Among the ferroelectric-gate memory transistors, Si-based ferroelectric-gate transistors have been studied most intensively for random access memory (FeRAM) applications and several reports have demonstrated good electrical properties.[3-5] However, the Si-based ferroelectric-gate memory transistors have not been put into practical use because they suffer from two major problems. The first problem is that it is very difficult to obtain a good interface between the ferroelectric layer and the silicon substrate due to the chemical reaction and interdiffusion during crystallization at high temperature.[6-8] The second problem involves charge mismatch leading to only partial polarization of a minor polarization-electric field (*P*-*E*) loop is used in the metal-ferroelectric-insulator-semiconductor (MFIS) structure. This fact results in a small memory window and high operation voltage (to increase the memory window). The charge mismatch problem can be overcome by using metal-ferroelectric-metal-insulator-semiconductor (MFMIS) structure.[7,8] However, such a complicated structure is not suitable for low-cost fabrication and for high integration. Because of these problems, it is difficult for Si-based ferroelectric-gate memory transistors to realize low-cost processing and high density implementation.

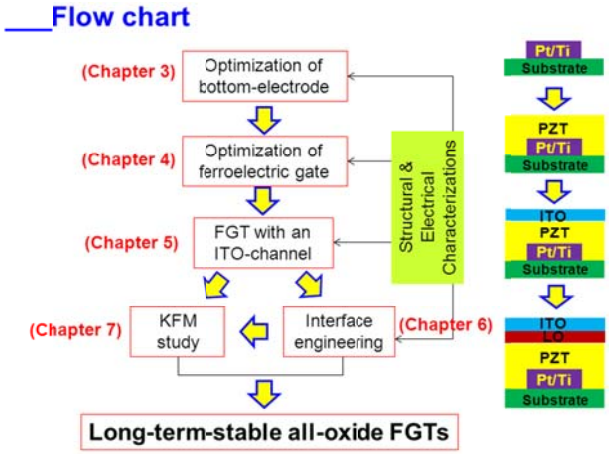
On the other hand, oxide-based ferroelectric-gate thin-film transistors (FGTs) could be one of the most promising candidates for low-cost, high-performance, highly integrated devices, because FGTs do not require a Si substrate and thus do not require complicated processing, because FGTs have a simple oxide-semiconductor/ferroelectric stacked structure and can be fabricated by only deposited films.[9-13] In addition, unlike Si-based ferroelectric-gate memory transistors, FGTs can use full ferroelectric polarization without any charge mismatch problem because a conductive oxide channel can be directly deposited on the ferroelectric-gate insulator. As mention above, this structure would increase memory window and improve retention properties.

## 2. Purpose

The first goal is to develop a new type of all-oxide ferroelectric-gate thin-film transistor (FGT) device with a simple semiconductor/ferroelectric stacked structure by using solution process instead of costly vacuum process while ensuring excellent transistor operation. The topics include fabrication and characterization of long-term-stable oxide based FGTs, and studying effects of each film quality and their interface on device performance. In particular, our experiments

start with an optimization of bottom electrode and ferroelectric layer. After that we demonstrate the operation of FGT devices with an oxide/ferroelectric structure stacked on this optimum gate insulator and electrode. For high performance FGT device, we propose solutions for a perfect semiconductor/ferroelectric heterostructure with good interface properties.

On the other hand, device physics of ferroelectric memories including dynamic operation and failure mechanism (i.e., poor retention, low switching speed, etc…) which is inevitable for optimization of the device, has not been understood well due to a lack of scientific characterization. In this dissertation, Kelvin probe force microscopy (KFM) study on operating FGT devices was carried out to understand the charge transportation as well as operational principle of the device, and to correlate the device features, namely structure and source/drain electrode materials, with its performance. In particular, the dependence of contact and channel resistances as well as field-effect mobility on the gate- and source/drain-bias is systematically analyzed based on parameters extracted from potential profiles and from FET theory. Additionally, effects of source/drain materials, device configuration, and film morphology on device performance are evaluated. Physics of carrier transport and carrier distribution depending on field-effect will be discussed. A flow chart of this dissertation is described in the figure.




## 3. Experimental results

### 3.1. Optimization of Pt and PZT thin films for ferroelectric-gate thin-film transistors

First of all, optimization of Pt and PZT thin films for FGTs was carried out. We have succeeded in preparing highly (111)-oriented polycrystalline Pt and PZT thin films on various types of substrate:

+ The deposition and characterization of Pt film were conducted as a function of sputtering conditions such as substrate temperature, argon working pressure, sputtering power, and substrate-target distance. We found that the dominant parameters in controlling the uniformity and crystallinity are the substrate temperature and Ar working pressure.

+ The orientation of sol-gel derived PZT film is strongly dependent on the bottom electrode and the annealing process. We pointed out that the formation of a $PbPt_x$ phase having close crystal structure to tetragonal PZT at PZT/Pt interface, which acts as a seed layer, during the intermediate annealing step (400 $^oC$) plays an important role on subsequent epitaxial-like growth of the PZT film. The obtained polycrystalline PZT film showed a dense structure and smooth surface. Further, highly (111)-oriented PZT film exhibited excellent electrical properties, i.e., high remnant polarization ($2P_r$ ~ 100 μC/cm$^2$), small coercive voltage ($2E_c$ ~ 300 kV/cm), and relatively low leakage current (~ $10^6$ A/cm$^2$ at 600 kV/cm).

### 3.2. Solution-processed indium-tin-oxide (ITO)-channel ferroelectric-gate thin-film transistors

Next, operation of solution-processed ITO-channel FGT device, which used the optimum Pt and PZT films, has been verified. The FGT device exhibited a typical n-type operation in a depletion mode. A relatively large “on/off” current ratio, an adequate memory window, and a large “on” current of $10^6$, 1.5 V, and 4 mA were obtained, respectively. In order to further improve the device performance, the effects of PZT and ITO layer thickness as well as ITO-annealing conditions (i.e., temperature, ambient, time) were systematically investigated. It was found that the device characteristics are very sensitive to the ITO annealing conditions or more specifically, carrier density. In order to realize a complete “off” state it is important to prepare thin enough ITO layer followed by relatively low annealing temperature (around 450 $^oC$).

However, the FGT device using ITO/PZT structure showed pronounced operation instability. This instability is most likely due to poor interface properties between the ITO and PZT layer due to the compositional interdiffusion. We

showed that an amorphous interlayer having a thickness of 7-10 nm exists at the ITO/PZT interface. In particular, Zr was segregated at the PZT surface, while Pb atoms were diffused into the ITO layer and that 10% of Pb was found in it. This interlayer must store a large amount of trapped charges altering the way of ferroelectric polarization to control the channel conductivity. Therefore, preventing the interdiffusion or reaction is one of the key factors to realize good interface properties of solution-processed ITO/PZT system for a high performance FGT device.

In order to solve the interdiffusion problem we proposed the use of a thin $La_2O_3$ (LO) film as a capping layer between the ITO and PZT layers. The fabricated ITO/LO/PZT structure exhibited stable operation with the extraordinarily high "on/off" current ratio and large memory window of $10^8$ and 3.5 V, respectively. An improved data retention time up to 1 day was also experimentally demonstrated. We showed that the LO layer not only prevent the interdiffusion but also stabilize the PZT surface structure. Furthermore, it was found that $La^{3+}$ ions diffused into the PZT layer and may substitute for $Pb^{2+}$ ions resulting in improved stability of PZT perovskite structure in terms of Pb volatility and formation of oxygen vacancies. Therefore, the interdiffusion was suppressed so that the device properties were improved greatly as a result of the good interface properties between the ITO and PZT layers. The obtained transistor properties in this work are better than most of the reported FGT devices in literatures.[9-13]

### 3.3. Kelvin probe force microscopy study on operating FGT devices

In parallel, we have developed Kelvin probe force microscope technique (KFM) that can be performed on operating devices and provide local, nanoscale information about device physics of the FGT device, which cannot be obtained by other techniques. KFM measurements were conducted for directly mapping surface potential distribution within the channel and correlating the surface potential with device structure as well as the film morphology. It is demonstrated that the measured potential reflects the electrostatic potential of the accumulation layer at the semiconductor/ferroelectric interface. The noticeable non-linearity of potential profiles observed near and over the "pinch-off" is directly associated with a spatially-dependent carrier density within the channel. In addition, the surface potential distribution was used to isolate the potential drops at the source/drain contacts and across the channel. We found that the contact and channel resistances decreased dramatically with increasing the gate bias but did not depend strongly on the source/drain bias, which is clearly related to the physics of electronic transport under field-effect doping. Further, we present data revealing gate bias and lateral field dependence of the field-effect mobility in the ITO channel. This study demonstrates that the utility of KFM for visualizing charge transport in operating FGT device and for correlating electrical behavior with device structure by comparison of surface potential and topographic map.

## 4. Conclusion and Prospect

We have succeeded in demonstrating operation of ferroelectric-gate thin-film transistor (FGT) fabricated by solution-process for the first time. Good transistor operation, which is comparable with or better than state-of-the-art vacuum-processed FGT devices, was verified with relatively large "on/off" current ratio and adequate memory window. Those results can be obtained by optimization of thin films and their interfaces including the bottom-gate electrode (Pt), ferroelectric-gate insulator (PZT), and semiconductor/ferroelectric (ITO/PZT) interface. We have solved one of the biggest issues of FGTs concerning the semiconductor/ferroelectric interface by the use of a lanthanum oxide (LO) thin film as a capping layer between the ITO and PZT layers. Based on these achievements we conclude that the solution process could be used instead of conventional vacuum processes for fabrication of oxide-based inorganic FGT devices. The success of such a solution processing would be a big step toward "total printing inorganic electronics" that could enable ultra-low-cost and low-energy fabrication of sophisticated inorganic memories and thin-film transistors.

In addition, we have developed Kelvin probe force microscopy technique that can be performed on operating FGT devices and provide local, nanoscale information about device physics of FGT and other devices that cannot be obtained withy other techniques. This characterization would provide bases for insight understanding and establishing device physics of the ferroelectric memories, for addressing device failure mechanism as well as for optimization of the devices.

## TABLE OF CONTENTS



### LIST OF PUBLICATIONS

1. P. T. Tue, T. Miyasako, B. N. Q. Trinh, J. Li, E. Tokumitsu, and T. Shimoda, "Optimization of Pt and PZT films for Ferroelectric-Gate Thin Film Transistors", Ferroelectrics, **405**:1 (2010) pp. 281-291.
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5. J. Li, H. Kameda, B. N. Q. Trinh, T. Miyasako, P. T. Tue, E. Tokumitsu, T. Mitani and T. Shimoda, "A low-temperature crystallization path for device-quality ferroelectric films", Appl. Phys. Lett., **97** (2010) pp. 102905-07.
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## Papers in preparation

1. P. T. Tue, B. N. Q. Trinh, T. Miyasako, P. V. Thanh, E. Tokumitsu, and T. Shimoda, "Lanthanum surface-modified lead zirconium titanate system for solution-processed ferroelectric-gate thin-film transistors".
2. P. T. Tue, T. Miyasako, B. N. Q. Trinh, E. Tokumitsu, and T. Shimoda, "Kelvin probe force microscopy study on operating ferroelectric-gate thin-film transistor".

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