An Algorithm for Post-Silicon Skew Tuning Based on Iterative Path Delay Testing

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As the development of LSI technologies advances from deep sub-micron to nano-meter, manufacturing process variations are becoming a more critical issue. The increase of the process variations can lead to timing errors in a digital circuit, and as a result, the yield of chip will be degraded seriously. On the other side, when we design LSIs with a redundant margin to make sure that the circuit satisfies the timing constraints, the performance of a chip is degraded. Possbile solutions to this problem are classified into two types, one is pre-silicon timing optimization and the other is post-silicon tuning.

Statistical Static Timing Analysis (SSTA) is a representative approach in the former. It calculates circuit delay statistically and tradeoffs the performance and the yield of chips based on the probability distribution function of parameter of the device such as gate and transistor. However, it is hard to get the correct distribution function and the performance of chips is underestimated. On the other hand, post-silicon tuning tries to tune a part of the circuit by observing the condition of the fabricated chip. One of the best methods for post-silicon tuning is deskew technique where delay values of the clock tree are tuned to satisfy the timing constraint.

One example of deskew technique uses programmable delay elements (PDEs) inserted on a clock distribution tree, and the clock arrival time to

each FF is adjusted by tuning PDE according to the real delays of individual fabricated chip. Problems arising from Post-Silicon tuning include circuit design for tunability enhancement and the procedure for tuning PDE from a set of test results, and the latter is our subject for study.

Being different from conventional methods which rely on the measurement of delay and the numerical computation of tuned delay of each PDE, our proposed method for tuning PDE repeats timing test and adjustment of PDE control values.

In this paper we target a combination circuit, and we assume that one PDE is inserted on the clock signal path of each FF so that we can tune the clock signal arrival time of each FF independently. Let $R_i \in \{0, 1, \ldots, 2^N - 1\}$ be the discrete control value of PDE_i which inserted before FF_i, and let $f_i(R_i)$ be generated delay value by PDE_i. $f_i(R_i)$ is also effected by the process variations, but $f_i(a) < f_i(b)$ for $a < b$ is assumed even after suffering process variations.

In order to search the correct value of every PDE, we define the relativity revised constraint graph (constraint graph) G. G is a weighted and directed graph, and each vertex represents each FF (PDE) in a circuit. A directed edge represents the timing constraint betweent FFs. Based on the result of timing test for the current PDE control value when the clock signal arrival time of the FF(FF_i) of one side of a signal propagation pass in the combination circuit have to be put off than the FF(FF_j) of another side, we set the color on edge(FF_j, FF_i) to be red. When it is not necessary, we set the color to be green. In addition to edge coloring, we will maintain a weight w_{ij} which indicates the lower bound of necessary difference value of $R_i - R_j$.

In the algorithm of searching the correct value of PDEs, first we build the constraint graph G and initialize it. Then the circuit is tested by timing test, each edge of G is colored with red or green and the value of w is updated depending on the result of timing test. Now we will check whether there exist positive-weight cycles in graph G. If there is one or more, the algorithm terminates with answering "no feasible set of PDE control values". If there is no positive-weight cycle in G, we regard the problem as the longest path problem of graph to find the discrete control value of each vertex which satisfies minimum necessary difference w of each

edge. When we got these values, we can set them to the circuit and do timing test again. We repeat these steps until all of timing violations are corrected.

Here we have the following theorem:

when the delay function $f_i(R_i)$ is linear for every PDE and has the same slope, if there exists one or more positive-weight cycles in the constraint graph G, there is no feasible set of PDE control values which satisfy every timing constraint.

Finally, our proposed method has been tested through computer simulations. In these simulations, hundreds of circuit instance having different path delay values were generated from each test circuit, and our proposed method was applied to each of those variants. ILP solution as well was computed for knowing exact solution whether each instance has a feasible set of PDE control value or not. Through those simulations, it has been verified that our proposed method always answer correctly if every PDE has the same delay slope with respect to the control value, but not for the case of different delay slopes or nolinear delay with respect to PDE control value. Algorithm improvement for the latter case is left as one of future works.